DS25Q4DN

3.3V 1G-bit ECC

Serial Flash Memory with 4KB Sectors, Standard, Dual and Quad I/O SPI & QPI

Documents title

3.3V 1Gb bit Serial Flash Memory with 4KB Sectors, Standard, Dual and Quad I/O SPI &QPI

Revision History

Revision No.	History	Draft date	Release date	Remark
0.0	Initial Draft	Mar.18.2025	Mar.25.2025	Preliminary
0.1	Add automotive 105°C P/N and update ICC1 typical value	Jul.14.2025	Jul.17.2025	
0.2	Update DTR max frequency and corresponding ICC3 value	Feb.05.2026	Feb.10.2026	

Datasheet can be modified without any notice!

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1. GENERAL DESCRIPTIONS

The DS25Q4DN (1G-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25 series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25uA standby current and 1µA for power-down. All devices are offered in space- saving packages.

The DS25Q4DN array is organized into 512K programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The DS25Q4DN has 32K erasable sectors and 2K erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The DS25Q4DN support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI) as well as Double Transfer Rate(DTR) : Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/RESET). SPI clock frequencies of up to 166MHz are supported allowing equivalent data rates of 332Mbits/s for Dual I/O and 664Mbits/s for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24/32-bit address, allowing true XIP (execute in place) operation.

Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Advanced Sector Protection mode can protect the content in memory through password. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 128-bit Unique Serial Number and 3x1024bytes Security Registers. Integrated ECC and CRC function intensify the data integrity.

2. FEATURES

- **New Family of SPI Flash Memories**
  - DS25Q4DN: 1G-bit /128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - DTR(Double Transfer Rate) Read
  - 3 or 4-Byte Address Mode
- **Highest Performance Serial Flash**
  - 166MHz Single, Dual/Quad SPI clocks
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
  - Burst Read with 16/32/64 Byte Wrap
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 16/32/64-Byte Wrap
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
- **High performance program/erase speed**
  - Page program time: 0.3ms typical
  - Sector erase time: 30ms typical / Industrial
    85ms typical / Automotive
  - Block Erase time: 0.15/0.22s typical
  - Chip erase time: 60 seconds typical
- **Data Integrity Check**
  - On-chip ECC (1-bit correction every 8-Byte)
  - CRC detects accidental changes to raw data
- **Low Power Consumption**
  - Full voltage range: 2.7-3.6V
  - 25µA typical standby current
  - 1µA typical deep power down current
- **Wide Temperature Range**
  - -40°C to +85°C/105°C /125°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- **Advanced Security Features**
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection
  - Advanced Sector Protection mode
  - 128-Bit Unique ID for each device
  - Support Serial Flash Discoverable Parameters (SFDP) signature
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 16-pin SOP 300-mil
  - 8-pad WSON 8x6-mm
  - 24Ball FBGA

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1. 16-pin SOP 300-mil

Figure 1a. Pin Configuration

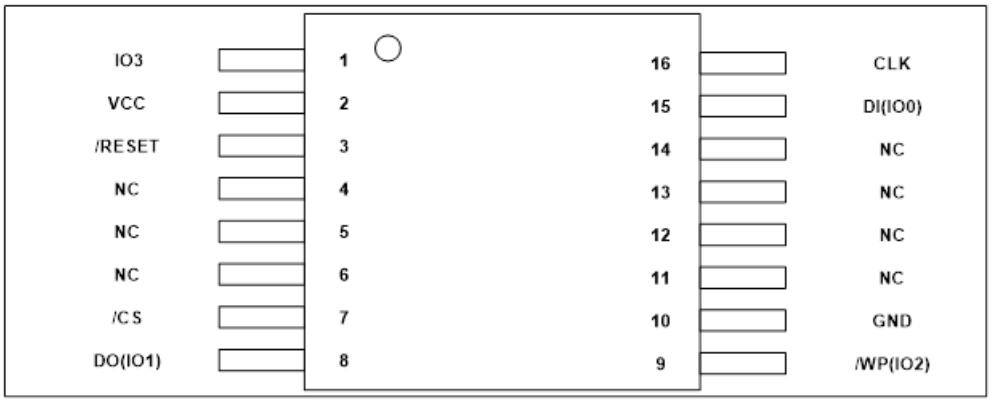


Table 1a. Pin Description

PIN NO.	PIN NAME	I/O	FUNCTION
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	/RESET	I	Reset Input
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO(IO1)	I/O	Data output (Data Input Output 1)
9	/WP(IO2)	I/O	Write Protection Input (Data Input Output 2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI(IO0)	I/O	Data Input (Data Input Output 0)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP functions are only available for Standard/Dual SPI.
3. If hardware reset function is not used, the separate hardware /RESET pin must be connected to VCC in system.
4. If /WP pin is not used, it must be driven high by host, or an external pull-up resistor must be placed on the PCB in order to avoid floating

3.2. BGA24

Figure 1b. Ball Configuration

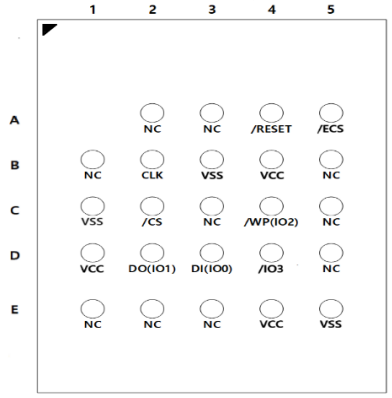


Table 1b. Ball Description

PIN NO.	PIN NAME	I/O	FUNCTION
A4	/RESET	I	Reset Input
A5	/ECS	O	ECC Correction Signal (Open Drain)
B2	CLK	I	Serial Clock Input
B3/C1/E5	VSS		Ground
B4/D1/E4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP(IO2)	I/O	Write Protection Input (Data Input Output 2)
D2	DO(IO1)	I/O	Data output (Data Input Output 1)
D3	DI(IO0)	I/O	Data Input (Data Input Output 0)
D4	IO3	I/O	Data Input Output 3
Others	N/C		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP functions are only available for Standard/Dual SPI.
3. If hardware reset function is not used, the separate hardware /RESET pin must be connected to VCC in system.
4. If /WP pin is not used, it must be driven high by host, or an external pull-up resistor must be placed on the PCB in order to avoid floating.
5. C1/E5 & D1/E4 are not mandatory connected to VSS/VCC in system, It is OK to leave them floating. Please contact us for detail check if any request about this.

3.3. 8-pad WSON 8x6-mm

Figure 1c. Pad Configuration

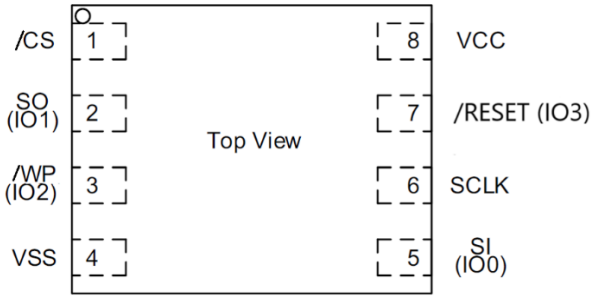


Table 1c. Pad Description

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)
6	CLK	I	Serial Clock Input
7	/RESET(IO3)	I/O	Reset Input (Data Input Output 3)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /RESET functions are only available for Standard/Dual SPI.
3. If /WP or /RESET pin is not used, it must be driven high by host, or an external pull-up resistor must be placed on the PCB in order to avoid floating.

Note: /CS must be driven high if chip is not selected. Please don't leave /CS floating any time after power is on for all package type.

4. PIN DESCRIPTIONS

4.1. Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down. If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2. Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The DS25Q4DN supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge ofCLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /RESET pin in WSON8X6 package becomes IO3.

4.3. Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP4, BP3, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-d for the pin configuration of Quad I/O operation.

4.4. Reset(/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin is the /RESET pin. When QE=1, /RESET function is not available for 8-pin configuration. For 16-pin and BGA24 packages, it is a separate /RESET pin.

4.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. BLOCK DIAGRAM

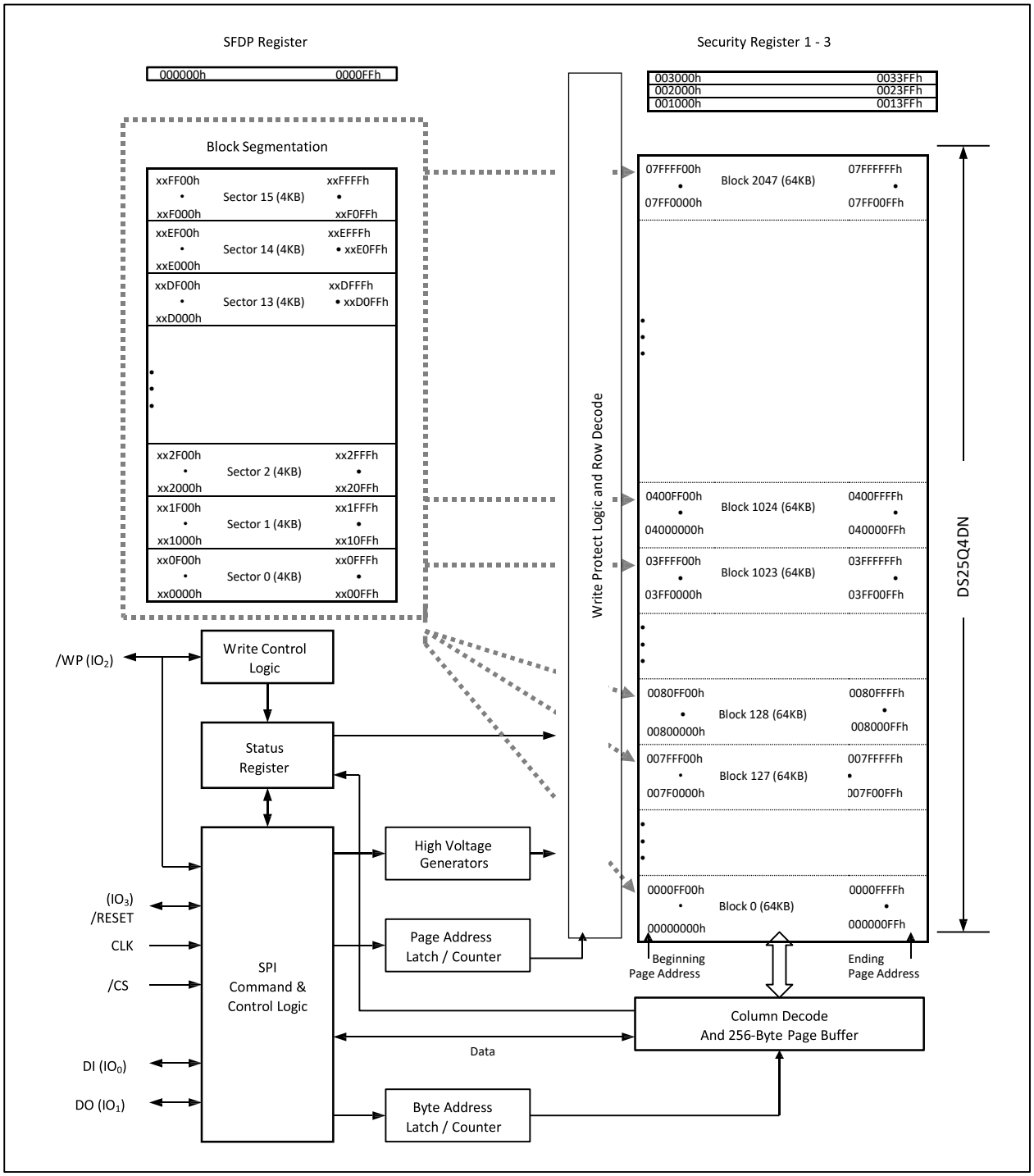


Figure 2. DS25Q4DN Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1. SPI / QPI Operations

6.1.1. Standard SPI Instructions

The DS25Q4DN is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2. Dual SPI Instructions

The DS25Q4DN supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non- speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3. Quad SPI Instructions

The DS25Q4DN supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)” and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /RESET pins(WSON8X6) become IO2 and IO3 respectively. Quad SPI instructions require the non- volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4. QPI Instructions

The DS25Q4DN supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/ Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /RESET (WSON8X6) pins become IO2 and IO3 respectively.

6.1.5. Quad SPI/ QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, DS25Q4DN introduces multiple DTR (Double Transfer Rate) Read instructions that support Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

6.1.6. 3-Byte / 4-Byte Address Modes

The DS25Q4DN provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128-Mbit data. To address more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256-Mbit to 32-Gbit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the DS25Q4DN can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the ADP Bit(S23) setting in status register 3. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP =1, the device will operate in 4-Byte Address Mode. The default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used.

DS25Q4DN also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Table for details.

6.1.7. Software Reset & Hardware /RESET pin

The DS25Q4DN can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 40uS (tRST) to reset. No command will be accepted during the reset period.

DS25Q4DN can also be configured to utilize a hardware /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input. (Figure 61)

If QE bit is set to 1, /RESET function will be disabled, the pin will become one of the four data I/O pins for 8 pin package types.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.

6.1.8. Ecc Function

The ECC Correction Signal (ECS#) pin is provided to the system hardware designers to determine the ECC status during any Read operation. The ECS# pin will be pulled low during any 8-Byte Read data output period in which an ECC event has occurred. ECS# pin can be used to represent SEC (Single Error Correction) event. ECC Correction Signal Output pin is an Open-Drain connection.

6.2. DATA PROTECTION

The DS25Q4DN provide the following data protection methods:

1，Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:

-Power-Up / Software Reset (66H+99H)

-Write Disable (WRDI)

-Write Status Register (WRSR) / Write Extend Address Register / Write Configuration Register / Write Password

-Page Program (PP) / Program Security Register

-Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE) / Erase Security Register

2，Software Protection Mode:

-The Block Protect bits (BP4, BP3, BP2, BP1 and BP0) define the section of the memory array that can be read but not changed.

-Individual Block Protection bit provides the protection selection of each individual block.

3，Hardware Protection Mode: WP# goes low to protect the Block Protect bits (BP4, BP3, BP2, BP1 and BP0) and the SRP bits (SRP1 and SRP0).

4，Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66H+99H).

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Extended Address Register, Write password, Write global freeze bit or Erase/Program Security Registers instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (BP[4:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Deep Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down and software reset instruction.

Table 2. DS25Q4DN Protected area size

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	2047	07FF0000h-07FFFFFFh	64KB	Upper 1/2048
0	0	0	1	0	2046 to 2047	07FE0000h-07FFFFFFh	128KB	Upper 1/1024
0	0	0	1	1	2044 to 2047	07FC0000h-07FFFFFFh	256KB	Upper 1/512
0	0	1	0	0	2040 to 2047	07F80000h-07FFFFFFh	512KB	Upper 1/256
0	0	1	0	1	2032 to 2047	07F00000h-07FFFFFFh	1MB	Upper 1/128
0	0	1	1	0	2016 to 2047	07E00000h-07FFFFFFh	2MB	Upper 1/64
0	0	1	1	1	1984 to 2047	07C00000h-07FFFFFFh	4MB	Upper 1/32
0	1	0	0	0	1920 to 2047	07800000h-07FFFFFFh	8MB	Upper 1/16
0	1	0	0	1	1792 to 2047	07000000h-07FFFFFFh	16MB	Upper 1/8
0	1	0	1	0	1536 to 2047	06000000h-07FFFFFFh	32MB	Upper 1/4
0	1	0	1	1	1024 to 2047	04000000h-07FFFFFFh	64MB	Upper 1/2
1	0	0	0	1	0	00000000h-0000FFFFh	64KB	Lower 1/2048
1	0	0	1	0	0 to 1	00000000h-0001FFFFh	128KB	Lower 1/1024
1	0	0	1	1	0 to 3	00000000h-0003FFFFh	256KB	Lower 1/512
1	0	1	0	0	0 to 7	00000000h-0007FFFFh	512KB	Lower 1/256
1	0	1	0	1	0 to 15	00000000h-000FFFFFh	1MB	Lower 1/128
1	0	1	1	0	0 to 31	00000000h-001FFFFFh	2MB	Lower 1/64
1	0	1	1	1	0 to 63	00000000h-003FFFFFh	4MB	Lower 1/32
1	1	0	0	0	0 to 127	00000000h-007FFFFFh	8MB	Lower 1/16
1	1	0	0	1	0 to 255	00000000h-00FFFFFFh	16MB	Lower 1/8
1	1	0	1	0	0 to 511	00000000h-01FFFFFFh	32MB	Lower 1/4
1	1	0	1	1	0 to 1023	00000000h-03FFFFFFh	64MB	Lower 1/2
X	1	1	X	X	ALL	00000000h-07FFFFFFh	128MB	ALL

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

There are two write protection methods provided on this device, "Block Protection (BP) mode" and "Advanced Sector Protection mode." The protection modes are mutually exclusive. The WPS bit in status register selects which protection mode enabled. If WPS=0 (factory default), BP mode is enabled and Advanced Sector Protection mode is disabled. If WPS=1, Advanced Sector Protection mode is enabled and BP mode is disabled. In advanced Sector Protection mode, individual Block/Sector can be locked or unlocked by command described in 8.2.48

Table 3. DS25Q4DN Individual Block Protection (WPS=1)

Block	Sector	Address range		Individual Block Lock Operation
2047	32767	07FF F000h	07FF FFFFh	**2048 Blocks** **Block Lock: 36H+Address Block**
	……	……	……	
	32752	07FF 0000h	07FF 0FFFh	

……	……	……	……	**Unlock: 39H+Address Read Block** **Read Lock: 3DH+Address** **Global Block Lock: 7EH** **Global Block Unlock: 98H**
……	……	……	……	
1022	16352~16367	03FE 0000h	03FE FFFFh	
……	……	……	……	
1	16~31	0001 0000h	0001 FFFFh	
0	15	0000 F000h	0000 FFFFh	
	……	……	……	
	0	0000 0000h	0000 0FFFh	

Notes:

Protection configuration: This bit is used to select which Write Protect scheme should be used.

Individual Block Protection bits are volatile lock bits. Each volatile bit corresponds to and provides volatile protection for an individual memory sector, all of them are protected when the device reset or power up.

The first and last sectors will have volatile protections at the 4KB sector level. Each 4KB sector in these sectors can be individually locked by volatile lock bits setting.

Individual Block Protection bits can further be protected by password protection mode.

To use this function, generally include two phrase: first, set the 64bit password through below steps

1. Make sure PWD bit in in configuration register equals 1(factory default) to enable password protection mode.
2. Issue Write Password command(28h) to set the password.
3. Read Password command(27h) can be issue to verify Write Password result. (option)

Before 2&3 steps, need make sure PWDLK bit in configuration register equals 1(factory default) so that password can be program and read out without locked.

4.Set PWDLK bit to 0 to lock the password, then password is successfully set and can not be programed and read out again.

Now, following steps can be used to modify individual block protection bits in password protection mode

1, Issue Unlock Password command(29h) with correct password to reset the global freeze bit(GFB) to 0. And Read Global Freeze Bit command(A7h) can be used to verify the Unlock Password command result.

2, Individual/Global Block/Sector Lock/Unlock command can be used to change the Individual Block Protection bits.

3.Issue Write Global Freeze Bit command(A6h) to set the global freeze bit(GFB) back to 1 so that the Individual Block Protection bits can not be modify without password to unlock again in password protection mode.

Please not that if password protection mode is disabled(PWD=0), the Global freeze bit(GFB) always equals 0, that means Individual/Global Block/Sector Lock/Unlock command can be used to change the Individual Block Protection bits in advanced Sector Protection mode without password protection mode, Unlock Password command(29h) has no effect on Global freeze bit, Read Password command(28h) can be accepted, but the read out password are all 0.. Write Global Freeze Bit command(A6h) can only write the Global freeze bit to 1 when password protection mode is enabled(PWD=1). Global freeze bit is used to protect the Individual Block Protection bits, which are volatile lock bits in locked status(=1). Global freeze bit is also equals 1 as freeze enable when power up if PWDLK=0, equals 0 as freeze disabled when power up if PWDLK=1.

PWD bit & PWDLK bit are Non-volatile OTP registers, so pay more attention to change the default value carefully. Make sure do not need password protection mode forever before set PWD bit to 0 to disable password protection mode; Make sure set password correctly and no need change anymore before set PWDLK bit to 0 to enable password lock.

6.3. INTEGRITY CHECK

The data storage and transmission errors will cause unexpected Flash device variation that makes a harmful impact on overall system functions. To prevent these errors, DS25Q4DN product provides advanced Data Integrity Check function. For the data storage and data transmission in the flash device, Data Integrity Check can check errors and correct them, allowing self-checking and preventing errors in advance.

The Data Integrity Check function includes two methods:
- ECC (Error Checking and Correcting): to prevent the data storage errors
- CRC (Cyclic Redundancy Check): to prevent the data transmission errors

The register data and software signals can also be used to associate the Data Integrity Check function to fully record the results of checking, and can also immediately feedback.

6.3.1. ECC (Error Checking and Correcting)

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device operation life and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In DS25Q4DN, every aligned 8-Byte data (A[2:0] = 0, 0, 0) stored in the memory array will be checked by the internal ECC engine using SEC (Single Error Correction) Hsiao Codes algorithm. With 8-Byte ECC data granularity, ECC calculation latency time can be minimized and highest level of data integrity can be preserved.

The default value of all memory data is FFH (Erased) when the device is shipped from the factory. A “Page Program (02H/12H)” or “Quad Page Program (32H/34H)” or “Extended Quad Page Program (C2H/3EH)” or Program security registers(42H) or Write password(28H) command can be used to program the user data into the memory array. When ECC is enabled (ECC=1 in Configuration Register), ECC calculation will be performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. It is necessary to program every page in aligned 8-Byte granularity so that ECC engine can store the correct ECC information.

ECC checking of a 8-Byte chunk will be disabled if double program (rewriting without erase), or rewrite a chunk(alternating of single bit, byte, or word) happens in that chunk. DPD bit in Extended Address Register bit6 shows whether some address of the last read out data have been double programmed or not. Once ECC checking of a chuck is disabled, it will not be re-activated until the sector, containing the ECC disabled chunk, is erased.

During data read operations, the internal ECC engine will check the ECC results stored in the spare area and apply necessary error correction or error detection to the main array data being read out. It is necessary to check the ECC Status Bits (SEC) in the Extended Address Register after every Read operation to see if the data read out contains one error or not. A Read operation can start from any Byte address and continue through the entire memory array, so it is not necessary to align the 8-Byte granularity boundary address to start a Read command.

Additional hardware monitoring of the ECC status can also be used to observe the ECC status in real time during any data output. When configured, the ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC event.

The SEC bit can be reset through anyone of the following situations:
- Sending a new Read Command
- Issuing Software Reset Command
- Hardware Reset
- Power-up cycle

6.3.2. ECS# (Error corrected Signal) Pin

The ECS# pin is a real time hardware signal to feedback the ECC correction status. The ECS# pin is designed as an open drain structure and a pull-up resistor (Rp) is required. In normal situation, the ECS# is kept on High-Z state. Once error correction begins, the ECS# pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing.

The ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC (Single Error Correction) event.

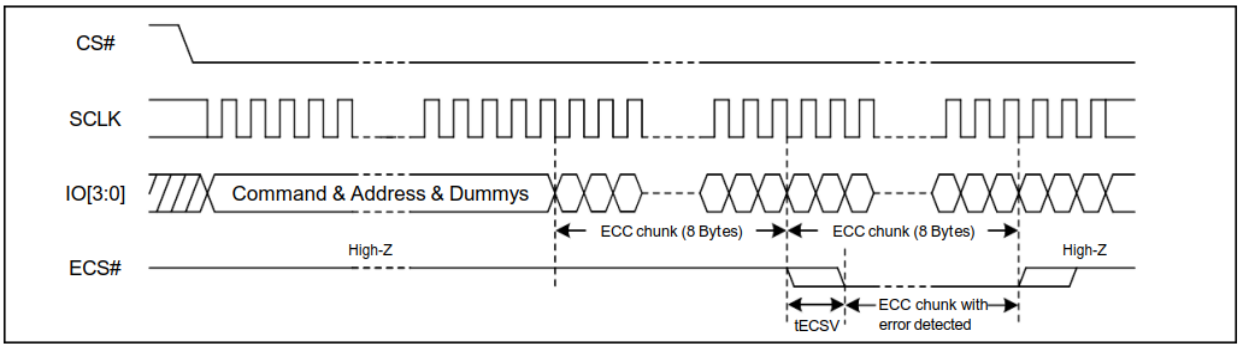


Figure 3. ECS# Timing

6.3.3. Parity Check (CRC)

The parity check function can only be operated in DTR read mode, and it is not supported in STR mode. The bit6~5 in the Configuration Register can set the parity check function.

For read operation after the Parity check function is enabled, the data CRC bit should be output by each CRC chunk unit. Otherwise, read CRC code might be error.

The CRC Chunk size can be configured as 16-Byte, 32-Byte, or 64-Byte by the Configuration Register setting. However, when the device enters the “Read with Wrap” mode, while the CRC function is also enabled, and the CRC Chunk size will be set to be identical with the Wrap Length (16-Byte, 32-Byte, or 64-Byte) by internal circuitry. Only when the device is not in the “Read with Wrap” mode, the original CRC Chunk size setting will be restored.

The data CRC Bytes are calculated by exclusive-OR on each I/O bus in the CRC chunk.

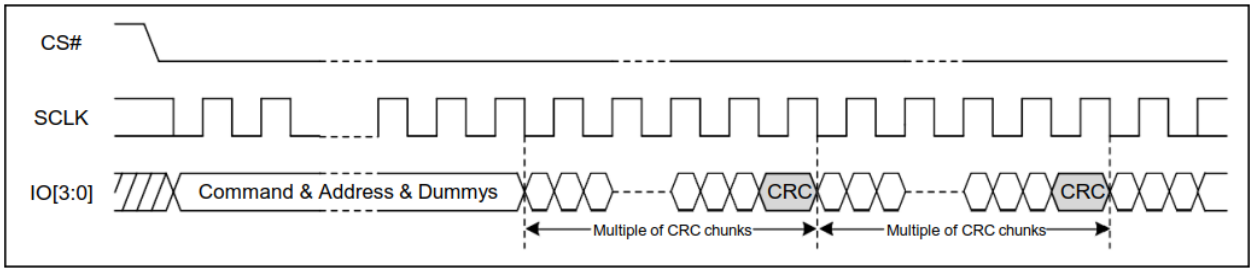


Figure 4. CRC Timing

7. REGISTERS

Three Status and Configuration Registers are provided for DS25Q4DN. The Read Status Register- 1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status and output driver strength. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, output driver strength and power- up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

7.1. Status Registers

Table 4 Status Register1

No.	Name	Description	Note	
S7	SRP0	Status Register Protect bit0	Non-volatile writable	volatile writable
S6	BP4	Block Protect bit	Non-volatile writable	volatile writable
S5	BP3			volatile writable
S4	BP2			volatile writable
S3	BP1			volatile writable
S2	BP0			volatile writable
S1	WEL	Write Enable Latch	Volatile, read only	
S0	BUSY/WIP	Erase/Write In Progress	Volatile, read only	

7.1.1. Erase/Write In Progress (BUSY/WIP) –*Volatile, Read Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Password or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register, Read Flag Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2. Write Enable Latch (WEL) –*Volatile, Read Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Extend Address Register, Write Password, Write global freeze bit or Erase/Program Security Register instruction.

7.1.3. Block Protect Bits (BP4, BP3, BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP4, BP3, BP2, BP1, BP0) are *Volatile/*non-volatile read/write bits in the status register (S6, S5, S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4. Status Register Protect (SRP1, SRP0) – *Volatile/Non-Volatile Writable*

The Status Register Protect bits (SRP1 and SRP0) are *Volatile*/non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 5 Status Register Protect

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written.

Notes:

1. When Non-Volatile SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change Volatile SRP1, SRP0 to (0, 0) state.
2. This feature is available upon special order. Please contact Dosilicon for details.

Table 6 Status Register2

No.	Name	Description	Note	
S15	SUS1	Erase Suspend Bit	Volatile, read only	
S14	WPS	Write Protection Select	Non-volatile writable	volatile writable
S13	LB3	Security Register Lock Bit	Non-volatile writable(OTP)	
S12	LB2			
S11	LB1			
S10	SUS2	Program Suspend Bit	Volatile, read only	
S9	QE	Quad Enable bit	Non-volatile writable	volatile writable
S8	SRP1	Status Register Protect bit1	Non-volatile writable	volatile writable

7.1.5. Erase/Program Suspend Status (SUS1, SUS2) – *Volatile, Read Only*

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/ Program Suspend (75H) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7AH) command, software reset (66H+99H) command, as well as a power-down, power-up cycle.

7.1.6. Write Protection Select (WPS) – *Volatile/Non-Volatile Writable*

There are two write protection methods provided on this device, "Block Protection (BP) mode" or "Advanced Sector Protection mode." The protection modes are mutually exclusive. The WPS bit selects which protection mode is enabled. If WPS=0 (factory default), BP mode is enabled and Advanced Sector Protection mode is disabled. If WPS=1, Advanced Sector Protection mode is enabled and BP mode is disabled.

7.1.7. Security Register Lock (LB3, LB2, LB1) – *Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 1024-Byte Security Register will become read-only permanently. LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits.

7.1.8. Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a *Volatile*/non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state, the /WP pin (and /RESET pin in WSON8X6) are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP (and /RESET pin in WSON8X6) functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. QE bit can not to set to 0 in QPI mode.

WARNING: If the /WP (or /RESET pin in WSON8X6) pins are tied directly to the power supply or ground during Standard/Dual SPI operation, the QE bit should never be set to a 1.

Table 7 Status Register3

No.	Name	Description	Note	
S23	ADP	Power up address mode	Non-volatile writable	
S22	DRV1	Output Driver Strength	Non-volatile writable	volatile writable
S21	DRV0			
S20	R	Reserved	N/A	volatile writable
S19	R			0
S18	ADS	Current address mode	Volatile, read only	
S17	EE	Erase Error bit	Volatile, read only	
S16	PE	Program Error bit	Volatile, read only	

7.1.9. Power up address mode (ADP) – *Non-Volatile Writable*

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0(factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.

7.1.10. Current address mode (ADS) – *Volatile, Read Only*

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

7.1.11. Erase Error (EE) – *Volatile, Read Only*

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. If the erase operation times out, the write enable latch bit is reset and the Erase error bit is set to 1. Error bits can be reset by Clear Flag Status Register command (71h)

Note: The EE bit can only be accessed when WIP=0 & SUS1=0.

7.1.12. Program Error (PE) – *Volatile, Read Only*

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. If the program operation times out, the write enable latch bit is reset and the program error bit is set to 1. Error bits can be reset by Clear Flag Status Register command (71h)

Note: The PE bit can only be accessed when WIP=0 & SUS2=0.

7.1.13. Output Driver Strength (DRV1 & DRV0) – *Volatile/Non-Volatile Writable*

The Oupput Driver Strength (DRV1 & DRV0) bits are used to determine the output driver strength for the Read operations.

Table 8 Output Driver Strength

DRV1	DRV0	Driver Strength
0	0	25%
0	1	50%
1	0	75%(default)
1	1	100%

7.1.14. Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

7.2. Configuration Registers

Table 9 Configuration Register

No.	Name	Description	Note	
C7	ECC	ECC	Non-volatile writable	volatile writable
C6	CRC1	64/32/16/disable(default)	Non-volatile writable	volatile writable
C5	CRC0			
C4	DC2	dummy cycle 6/8/10(default)/12/14/16/NA/NA	Non-volatile writable	volatile writable
C3	DC1			
C2	DC0			
C1	PWDLK	Password lock	Non-volatile writable (OTP)	
C0	PWD	Password enable/disable	Non-volatile writable (OTP)	

7.2.1. ECC- *Volatile/Non-Volatile Writable*

ECC (Error Correction Codes) Status Bit is used to configuration the ECC function for prevent the data storage errors. ECC equals 1 as enable(default).

7.2.2. CRC1 & CRC0- *Volatile/Non-Volatile Writable*

CRC1 & CRC0 is used to configure the number of CRC code byte, CRC function is disabled by default

CRC0 and CRC1 (Cyclic Redundancy Check bit) Status bits are used to configure the CRC chunk size for prevent the data transmission errors.

Table 10 CRC1 & CRC0

Function	CRC1	CRC0	Definitions
CRC configuration	1	1	CRC Disabled(Default)
	1	0	16 Byte CRC
	0	1	32 Byte CRC
	0	0	64 Byte CRC

7.2.3. Dummy cycle (DC0 & DC1 & DC2) –*Volatile/Non-Volatile Writable*

DC0&DC1&DC2 bits are used to set Dummy cycle corresponding to read frequency. (defined in Dummy Cycle and Frequency Table)

The default number of dummy clocks is 10. The number of dummy clocks for BBH/EBH/ECH/EDH/EEH at SPI mode and 0BH/0CH/EBH/ECH/EDH/EEH/5AH/4BH/48H at QPI mode will be set by DC bits in Configuration register, the number of dummy clocks can be configured as either 6/8/10/12/14/16 (default = 10).

Table 11 Dummy cycle configuration(SOP16/BGA24/WSON6X8)

Number of Dummy Clock Cycle	Quad I/O FAST READ		QPI DTR
	STR	DTR	
6	133	84	84
8	166	90	90
10	166	90	90
12	166	90	90
14	166	90	90
16	166	90	90

Note: If STR frequency exceeds 166MHz or DTR frequency exceeds 90MHz, please contact us.

DC2 – DC1 – DC0	DUMMY CLOCKS
0 0 0	6
0 0 1	8
0 1 0	10
0 1 1	12
1 0 0	14
1 0 1	16
1 1 0	16
1 1 1	10(default)

7.2.4. PWDLK- *Non-Volatile Writable(OTP)*

PWDLK is Password lock bit which can be set to 0 to enable Password lock function by user only one time(OTP), it is equals to 1 by factory default disabled so that user can access.

PWDLK bit is Non-volatile OTP registers, so pay more attention to change the default value carefully. Make sure set password correctly and no need change anymore before set PWDLK bit to 0 to enable password lock.

7.2.5. PWD -- *Non-Volatile Writable(OTP)*

PWD bit if used for Password enable/disable function which can be set to 0 to disable password protection mode by user only one time(OTP), it is equals to 1 by factory default enabled.

PWD bit is Non-volatile OTP registers, so pay more attention to change the default value carefully. Make sure do not need password protection mode forever before set PWD bit to 0 to disable password protection mode.

7.3. Flag Status Registers

Table 12 Flag Status Register

MILAN flag status register			
No.	**Bit Name**	**Description**	**Note**
F7	RY/BY#	Ready/Busy#	Volatile, read only
F6	SUS1	Erase Suspend	Volatile, read only
F5	EE	Erase Error bit	Volatile, read only
F4	PE	Program Error bit	Volatile, read only
F3	Reserved	Reserved	Volatile, read only
F2	SUS2	Program Suspend	Volatile, read only
F1	PTE	Protection Error bit	Volatile, read only
F0	ADS	Current Address Mode	Volatile, read only

7.3.1. Ready/Busy# (RY/BY#) -- *Volatile, Status-Only*

The RY/BY# bit is a read only bit that indicates busy or idle state. Indicates whether one of the following command cycles is in progress: Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Password or Erase/Program Security Register

This bit has opposite meaning and effect with BUSY bit in status register. SUS1/SUS2/PE/EE/ADS bit in Flag status register have the same meaning and effect with which have the same name described above already.

7.3.2. Protection Error (PTE) -- *Volatile, Status-Only*

The PTE bit is a read only bit that indicates a program or erase failure. Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space. PTE is cleared to "0" after program or erase operation resumes.

7.4. Extended Address Register

Table 13 Extended Address Register

No.	Name	Description	Note	
EA7	SEC	Single Error Bit 0 = No ECC events 1 = ECC events	Volatile, read only	
EA6	Reserved	Reserved	Non-volatile writable	
EA5	DPD	Double programmed without ECC protection in last read out data 1 = No ECC protection 0 = ECC protection	Volatile, read only	
EA4	Reserved	Reserved	Non-volatile writable	

EA3	A27	A27	Volatile writable	
EA2	A26	A26	Volatile writable	
EA1	A25	A25	Volatile writable	
EA0	A24	A24	Volatile writable	

7.4.1. Single Error Bit (SEC) -- *Volatile, Status-Only*

SEC (Single Error Correction) Status bit is used to show the ECC results for the last Read operation. SEC bit will be cleared to 0 once the device accepts a new Read command.

Table 14 SEC Definition

SEC	Definition
0	No ECC events in all aligned 8-Byte granularities
1	SEC events in single or multiple 8-Byte granularities, and the data is OK to use. (Unless it contains more than one odd bit errors in 8-Byte granularity)

7.4.2. Double programmed without ECC protection (DPD)-- -- *Volatile, Status-Only*

DPD Status bit is used to show whether some address of last read out data have been double programmed or not, if yes, DPD will be set to 1 that means ECC protection disabled for some aligned 8-Byte data in the latest read command.

7.4.3. A27/A26/A25/A24-- -- *Volatile, Status-Only*

A27/A26/A25/A24 are the extend address bit used in 3-byte address mode for 2Gb/1Gb/512Mb/256Mb density product .

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the DS25Q4DN instructions that are fully controlled through the SPI bus (see Instruction Set Table in 8.1.2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the DS25Q4DN instructions that are fully controlled through the SPI bus (see Instruction Set Table in 8.1.3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in chapter in 8.2. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1. Device ID and Instruction Set Tables

8.1.1. Manufacturer and Device Identification

DS25Q4DN

Table 15 ID Definition

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	E5	30	1B
90H	E5		1A
ABH			1A

8.1.2. Instruction Set Table (Standard/Dual/Quad SPI Instructions)

Standard/Quad SPI Command Name	Command	Address total bytes	byte1	byte2	byte3	byte4	Dummy clock	Data byte
Write Enable	06H	0					0	0
Write Disable	04H	0					0	0
Read Status Register-1	05H	0					0	1 to ∞
Read Status Register-2	35H	0					0	1 to ∞
Read Status Register-3	15H	0					0	1 to ∞
Write Status Register-1&2	01H	0					0	1 to ∞
Write Status Register-2	31H	0					0	1 to ∞
Write Status Register-3	11H	0					0	1 to ∞
Volatile SR/CR write Enable	50H	0					0	0
Read Data	03H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to ∞
4-Byte Read Data Bytes	13H	4	ADD1	ADD2	ADD3	ADD4	0	1 to ∞
Fast Read	0BH	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
4-Byte Read Data Bytes at Higher Speed	0CH	4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
Dual Output Fast Read	3BH	3(4)	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
Quad Output Fast Read	6BH	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
4-Byte Quad Output Fast Read	6CH	4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
Dual I/O Fast Read	BBH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
Quad I/O Fast Read	EBH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
4-Byte Quad I/O Fast Read	ECH	4	ADD1	ADD2	ADD3	ADD4	6/8/10/12/14/16 Note1/2	1 to ∞
DTR Quad IO read	EDH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
4-Byte Quad I/O DTR Fast Read	EEH	4	ADD1	ADD2	ADD3	ADD4	6/8/10/12/14/16 Note1/2	1 to ∞
Set Burst with Wrap	77H	4	Dummy	Dummy	Dummy	W7-W0	0	1 to ∞
Page Program	02H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Page Program	12H	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
Quad Page Program	32H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Quad Page Program	34H	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
Extended Quad Page Program	C2H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Extended Quad Page Program	3EH	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
Sector Erase	20H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0

Block Erase (32K)	52H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Block Erase (64K)	D8H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
4-byte sector erase	21H	4	ADD1	ADD2	ADD3	ADD4	0	0
4-byte BLK32 erase	5CH	4	ADD1	ADD2	ADD3	ADD4	0	0
4-byte BLK64 erase	DCH	4	ADD1	ADD2	ADD3	ADD4	0	0
Chip Erase	C7/60H	0					0	0
Read Manufacturer/Device ID	90H	3	00H	00H	00H	(MID7-MID0)	0	1 to ∞
Read Manufacturer/Device ID Quad IO	94H	3	00H	00H	00H		8	(MID7-MID0)
Read Identification	9FH	0	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)		0	1 to ∞
Read Serial Flash Discoverable Parameter	5AH	3	00H	00H	00H		8	1 to ∞
Read Unique ID	4BH	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to 128bit
Erase Security Registers	44H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Program Security Registers	42H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Read Security Registers	48H	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Enable Reset	66H	0					0	0
Reset	99H	0					0	0
Program/Erase Suspend	75H	0					0	0
Program/Erase Resume	7AH	0					0	0
Deep Power-Down	B9H	0					0	0
Release From Deep Power-Down	ABH	0					0	0
Release From Deep Power-Down and Read Device ID	ABH	3	Dummy	Dummy	Dummy	ID7-ID0	0	1 to ∞
Enable QPI	38H	0					0	0
Read Flag Status Register	70H	0					0	1 to ∞
Clear Flag status Register	71H	0					0	0
Read Configuration Register	B5H	0					0	1 to ∞
Read Extended Address Register	C8H	0					0	1 to ∞
Write Configuration Register	B1H	0					0	1
Write Extended Address Register	C5H	0					0	1
Enable 4-Byte Address Mode	B7H	0					0	0
Disable 4-Byte Address Mode	E9H	0					0	0
Individual Block/Sector Lock	36H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Individual Block/Sector Unlock	39H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Read Individual Block/Sector Lock	3DH	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1

Global Block/Sector Lock	7EH	0					0	0
Global Block/Sector Unlock	98H	0					0	0
read password	27H	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to 64bit
write password	28H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 64bit
unlock password	29H	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to 64bit
read global freeze bit	A7H	0					0	1
write global freeze bit	A6H	0					0	1

8.1.3. Instruction Set Table (QPI Instructions)

Standard/Quad SPI	**Command**	**Address**					**Dummy clock**	**Data byte**
Command Name		**total bytes**	**byte1**	**byte2**	**byte3**	**byte4**		
Write Enable	06H	0					0	0
Write Disable	04H	0					0	0
Read Status Register-1	05H	0					0	1 to ∞
Read Status Register-2	35H	0					0	1 to ∞
Read Status Register-3	15H	0					0	1 to ∞
Write Status Register-1&2	01H	0					0	1 to ∞
Write Status Register-2	31H	0					0	1 to ∞
Write Status Register-3	11H	0					0	1 to ∞
Volatile SR/CR write Enable	50H	0					0	0
Fast Read	0BH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
4-Byte Read Data Bytes at Higher Speed	0CH	4	ADD1	ADD2	ADD3	ADD4	6/8/10/12/14/16 Note1/2	1 to ∞
Quad I/O Fast Read	EBH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
4-Byte Quad I/O Fast Read	ECH	4	ADD1	ADD2	ADD3	ADD4	6/8/10/12/14/16 Note1/2	1 to ∞
DTR Quad IO read	EDH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
4-Byte Quad I/O DTR Fast Read	EEH	4	ADD1	ADD2	ADD3	ADD4	6/8/10/12/14/16 Note1/2	1 to ∞
Page Program	02H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Page Program	12H	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
Sector Erase	20H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Block Erase (32K)	52H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Block Erase (64K)	D8H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
4-byte sector erase	21H	4	ADD1	ADD2	ADD3	ADD4	0	0
4-byte BLK32 erase	5CH	4	ADD1	ADD2	ADD3	ADD4	0	0
4-byte BLK64 erase	DCH	4	ADD1	ADD2	ADD3	ADD4	0	0

Chip Erase	C7/60H	0					0	0
Set Read Parameters	C0H	1	P7-P0				0	0
Read Manufacturer/Device ID	90H	3	00H	00H	00H	(MID7-MID0)	0	1 to ∞
Read Identification	9FH	0	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)		0	1 to ∞
Read Serial Flash Discoverable Parameter	5AH	3	00H	00H	00H		6/8/10/12/14/16 Note1/2	1 to ∞
Read Unique ID	4BH	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to 128bit
Erase Security Registers	44H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Program Security Registers	42H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Read Security Registers	48H	3(4)	ADD1	ADD2	ADD3	(ADD4)	6/8/10/12/14/16 Note1/2	1 to ∞
Enable Reset	66H	0					0	0
Reset	99H	0					0	0
Program/Erase Suspend	75H	0					0	0
Program/Erase Resume	7AH	0					0	0
Deep Power-Down	B9H	0					0	0
Release From Deep Power-Down	ABH	0					0	0
Release From Deep Power-Down and Read Device ID	ABH	3	Dummy	Dummy	Dummy	ID7-ID0	0	1 to ∞
Disable QPI	FFH	0					0	0
Read Flag Status Register	70H	0					0	1 to ∞
Clear Flag status Register	71H	0					0	0
Read Configuration Register	B5H	0					0	1 to ∞
Read Extended Address Register	C8H	0					0	1 to ∞
Write Configuration Register	B1H	0					0	1
Write Extended Address Register	C5H	0					0	1
Enable 4-Byte Address Mode	B7H	0					0	0
Disable 4-Byte Address Mode	E9H	0					0	0
Individual Block/Sector Lock	36H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Individual Block/Sector Unlock	39H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Read Individual Block/Sector Lock	3DH	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1
Global Block/Sector Lock	7EH	0					0	0
Global Block/Sector Unlock	98H	0					0	0
read password	27H	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to 64bit

write password	28H	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 64bit
unlock password	29H	3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to 64bit
read global freeze bit	A7H	0					0	1
write global freeze bit	A6H	0					0	1

NOTE1: M7-0 is counted for dummy clocks.

NOTE2:

The number of dummy clocks for BBH/EBH/ECH/EDH/EEH at SPI mode and 0BH/0CH/EBH/ECH/EDH/EEH/5AH/4BH/48H at QPI mode will be set by DC bits in Configuration register, the number of dummy clocks can be configured as either 6/8/10/12/14/16 (default = 10).

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0H)” instruction can be used to configure the number of bytes of “Wrap Length” for “Quad I/O Fast Read (EBH/ECH)” and “DTR Fast Read Quad I/O (EDH/EEH)” instruction. In Standard SPI mode, the “Set Read Parameters (C0H)” instruction is not accepted, Set Burst with Wrap (77h) instruction can be used to configure the number of bytes of “Wrap Length” for “Quad I/O Fast Read (EBH/ECH)” and “DTR Fast Read Quad I/O (EDH/EEH)” instruction.

8.2. Instruction Descriptions

8.2.1. Enable 4-Byte Mode (B7H)

The Enter 4-Byte Address Mode instruction (Figure 5) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “B7h” into the DI pin and then driving /CS high. After sending the Enable 4-Byte Mode command, the ADS bit (FS0/S18) will be set to 1 to indicate the 4-Byte address mode has been enabled.

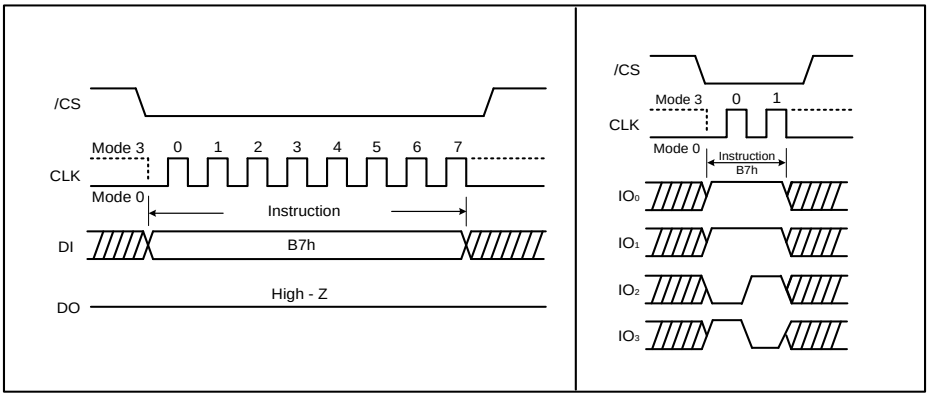


Figure 5 Enable 4-Byte Mode Sequence Diagram (SPI/QPI mode)

8.2.2. Disable 4-Byte Mode (E9H)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction (Figure 6) will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “E9h” into the DI pin and then driving /CS high. After sending the Disable 4-Byte Mode command, the ADS bit (FS0/S18) will be clear to be 0 to indicate the 4-Byte address mode has been disabled.

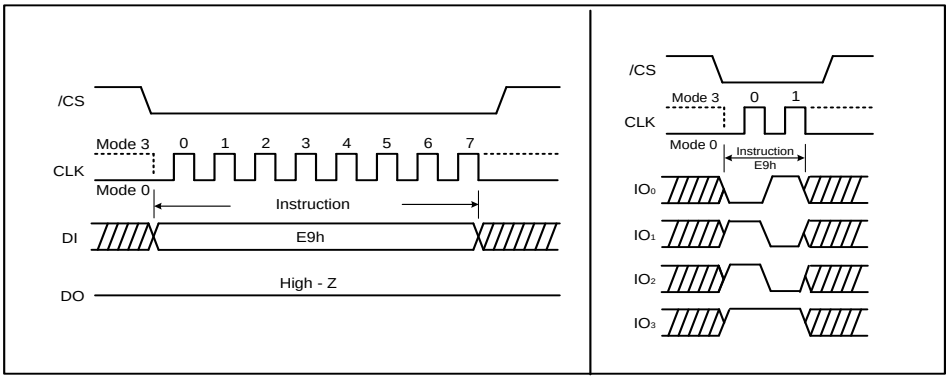


Figure 6 Exit 4-Byte Mode Sequence Diagram (SPI/QPI mode)

8.2.3. Write Enable (06h)

The Write Enable instruction (Figure 7) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Extended Address Register, Write password, Write global freeze bit or Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

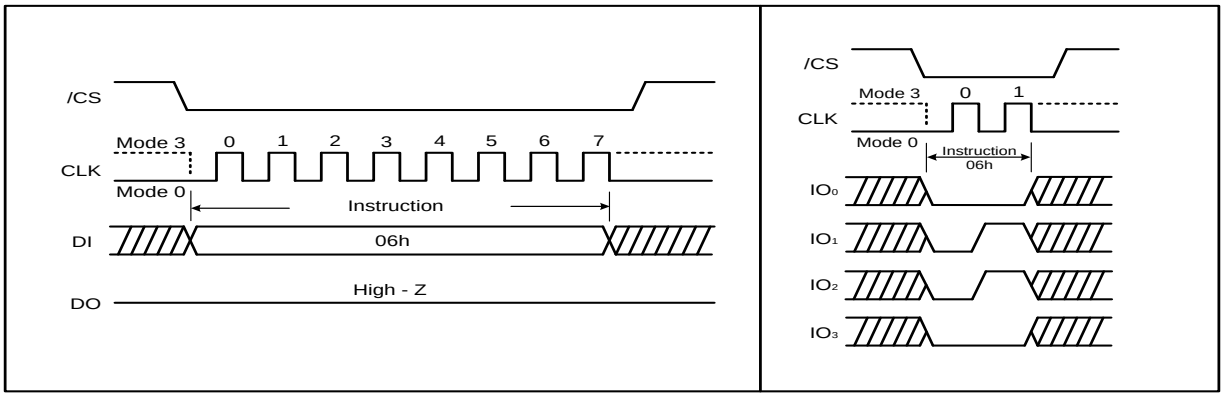


Figure 7. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

8.2.4. Write Enable for Volatile Status/Configuration Register (50h)

The non-volatile Status/Configuration Register bits described in section 7 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status/Configuration Register non-volatile bits. To write the volatile values into the Status/ Configuration Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status/Configuration Register (01h/31h/11h/B1h) instruction. Write Enable for Volatile Status/Configuration Register instruction (Figure 8) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status/Configuration Register instruction to change the volatile Status/Configuration Register bit values.

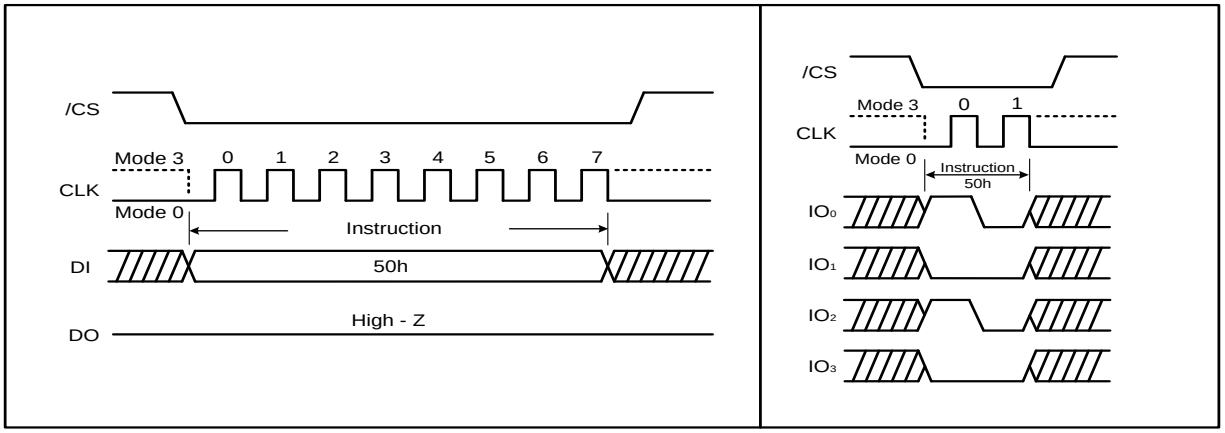


Figure 8. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

8.2.5. Write Disable (04h)

The Write Disable instruction (Figure 9) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Extended Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Configuration Register, Write Extended Address Register, Write password, Write global freeze bit, Erase/Program Security Registers or Reset instruction.

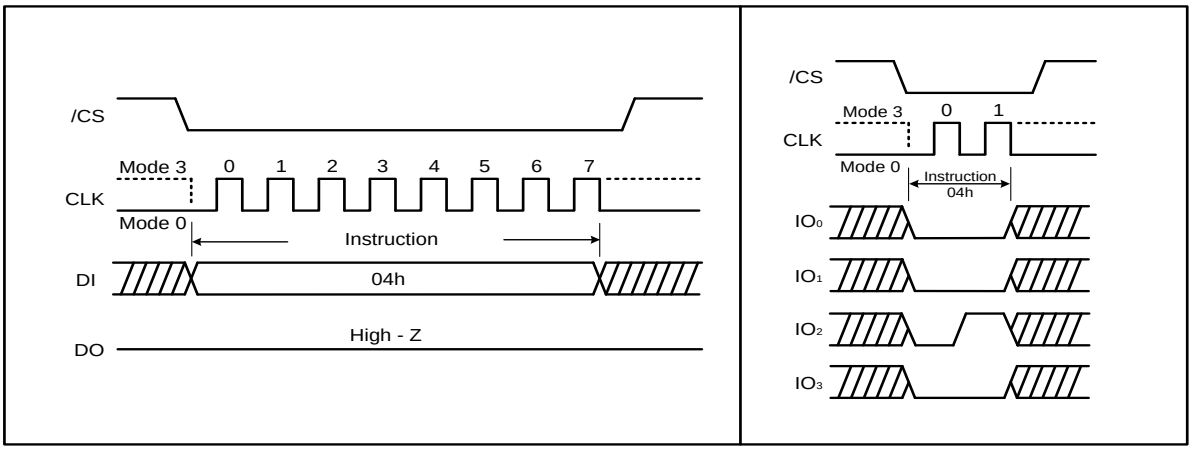


Figure 9. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

8.2.6. Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; WPS, LB[3:1], QE, SRP1 in Status Register-2; ADP, DRV in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non- volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 10a & 10b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL (See AC Characteristics).

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 7 for Status Register descriptions.

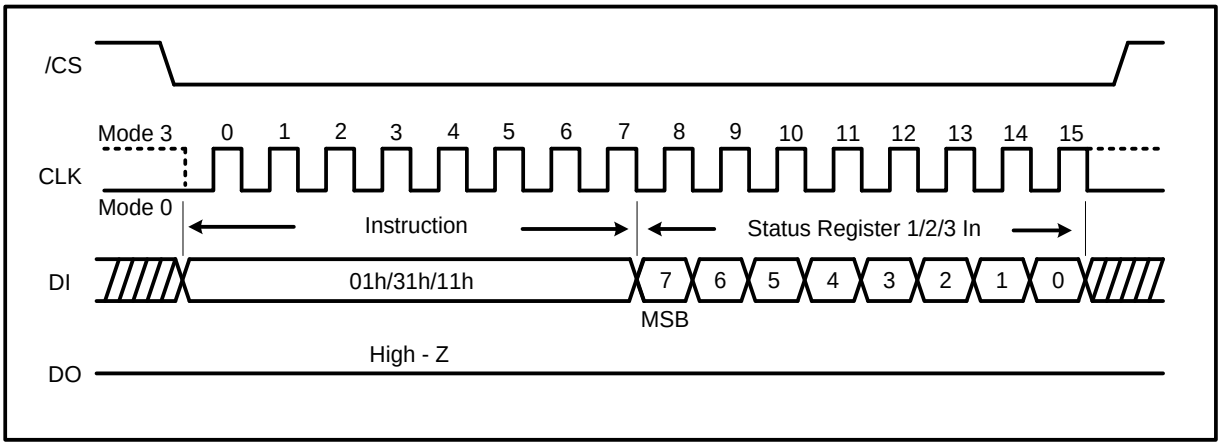


Figure 10a. Write Status Register-1/2/3 Instruction (SPI Mode)

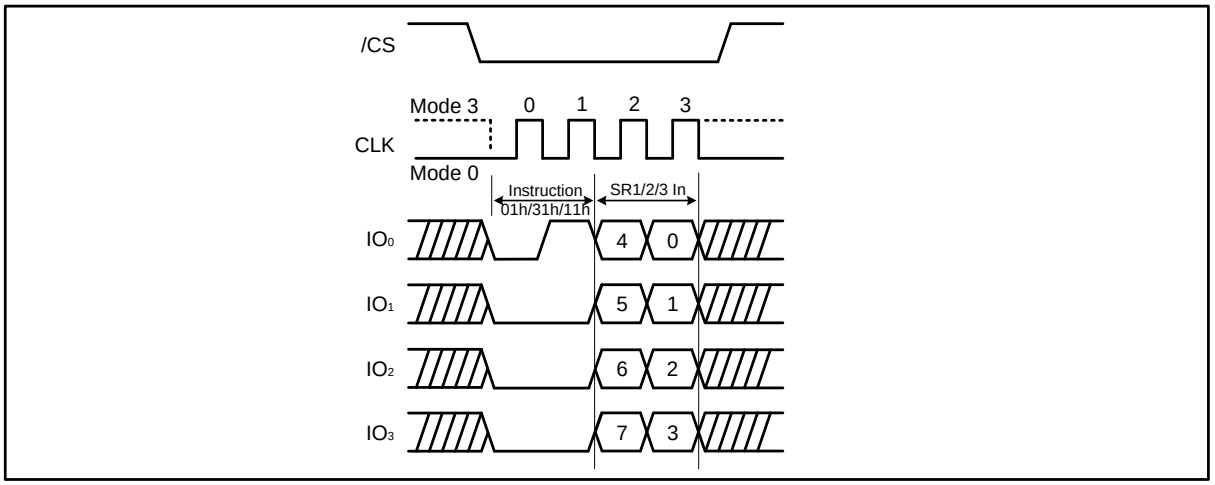


Figure 10b. Write Status Register-1/2/3 Instruction (QPI Mode)

The DS25Q4DN is also backward compatible to Dosilicon's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 10c & 10d. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected.

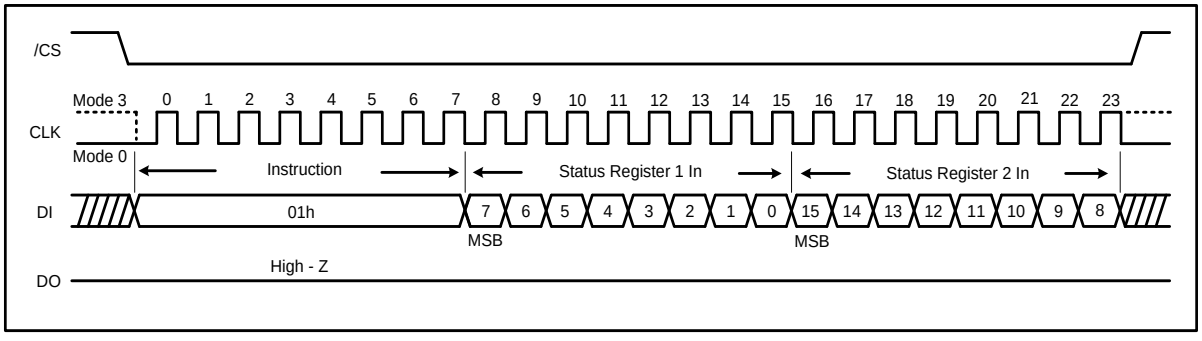


Figure 10c. Write Status Register-1/2 Instruction (SPI Mode)

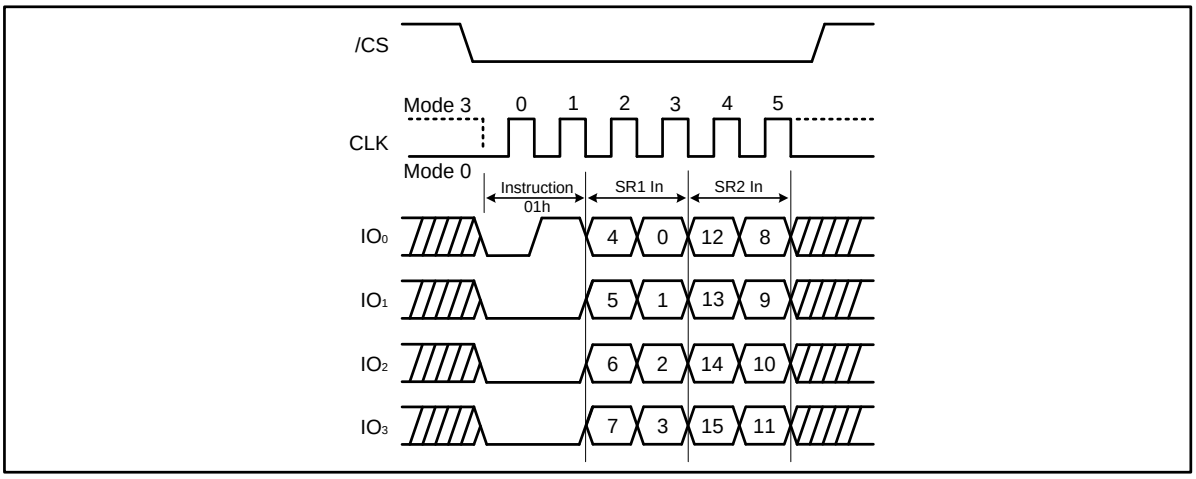


Figure 10d. Write Status Register-1/2 Instruction (QPI Mode)

8.2.7. Write Nonvolatile/Volatile Configuration Register (B1H)

The Write Nonvolatile/Volatile Configuration Register (WRCR) command allows new values to be written to the Nonvolatile/Volatile Configuration Register. Before it can be accepted, a Write Enable (WREN) or Write Enable for Volatile Status Register(50h) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

CS# must be driven high after the data Byte has been latched in. If not, the Write Configuration Register (WRCR) command is not executed. As soon as CS# is driven high, the self-timed Write Configuration Register cycle (whose duration is tW for B1H) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed Write Configuration Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

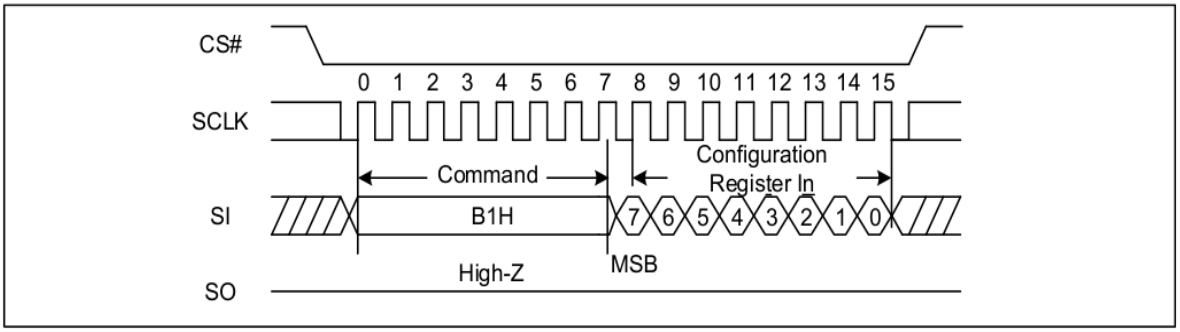


Figure 11a Write Nonvolatile/Volatile Configuration Register Sequence Diagram (SPI)

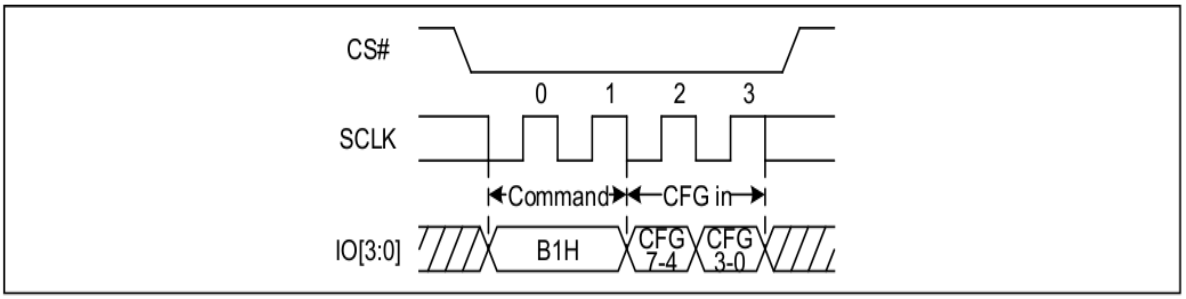


Figure 11b Write Nonvolatile/Volatile Configuration Register Sequence Diagram (QPI)

8.2.8. Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th Byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06H) instruction must previously have been executed for the device to accept the Write Extended Address Register

instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "C5H", and then writing the Extended Address Register data Byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Bit is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), command with address input of A31-A24 will not replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

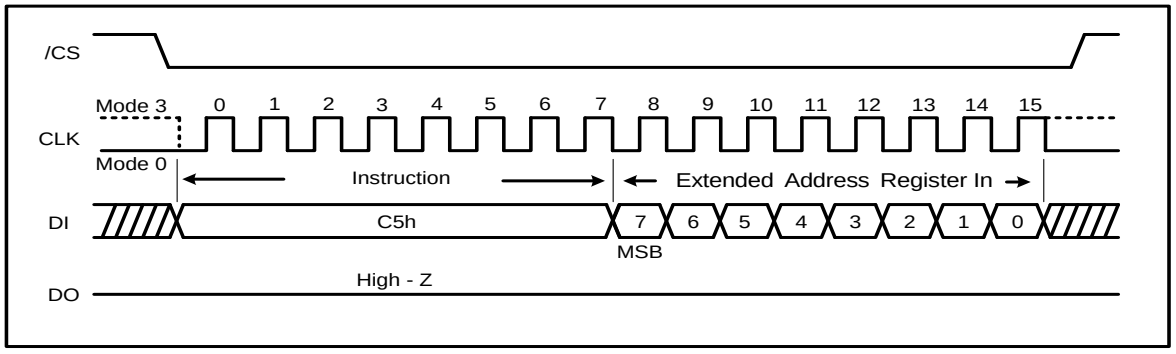


Figure 12a Write Extended Address Register Sequence Diagram (SPI)

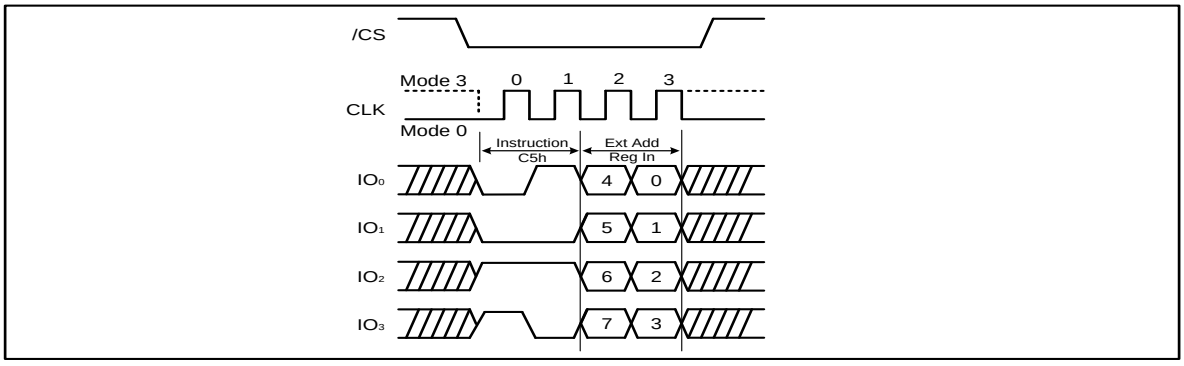


Figure 12b Write Extended Address Register Sequence Diagram (QPI)

8.2.9. Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code "05h" for Status Register-1, "35h" for Status Register-2 or "15h" for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 13. Refer to section 7 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 13. The instruction is completed by driving /CS high.

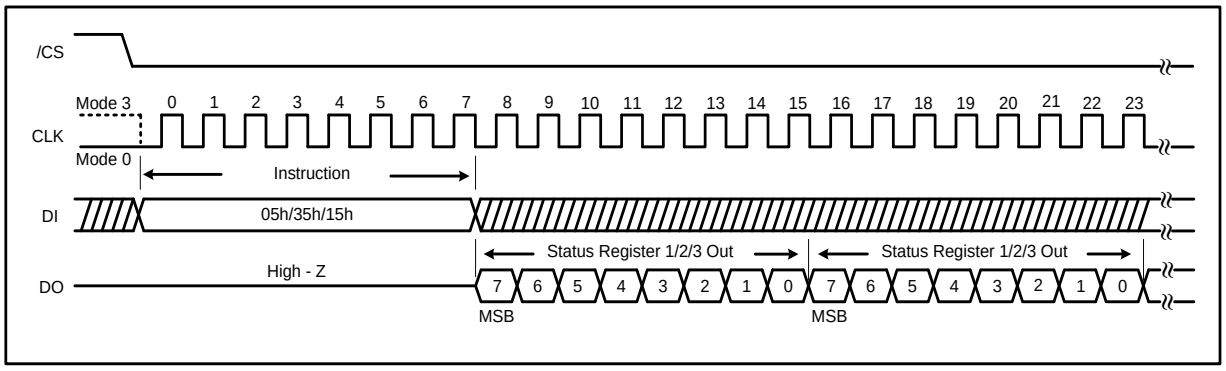


Figure 13a. Read Status Register Instruction (SPI Mode)

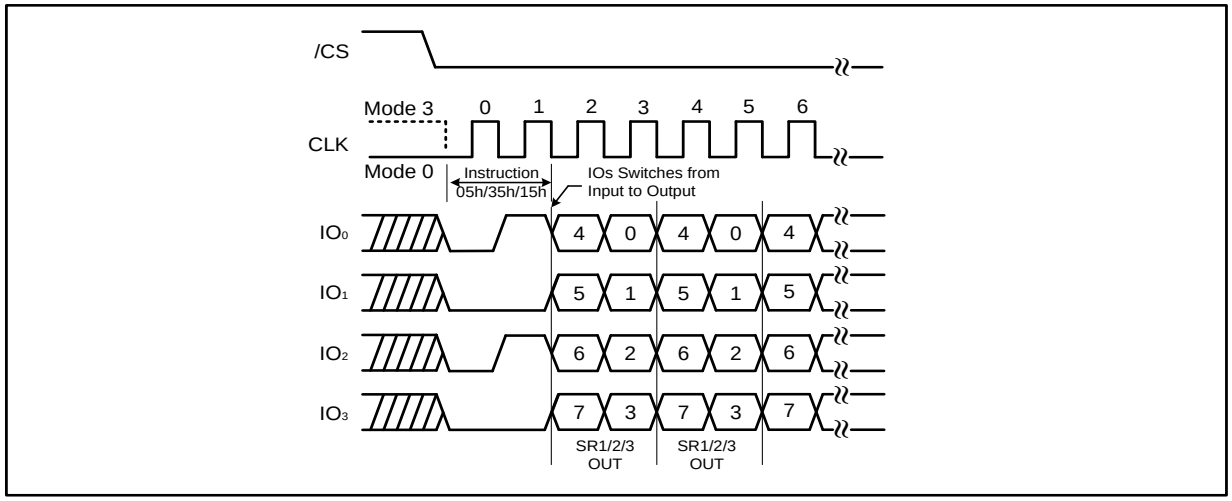


Figure 13b. Read Status Register Instruction (QPI Mode)

8.2.10. **Read Flag Status Register (70H)**

The Read Flag Status Register command is for reading the Flag Status Register. The Flag Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is also possible to read the Flag Status Register continuously.

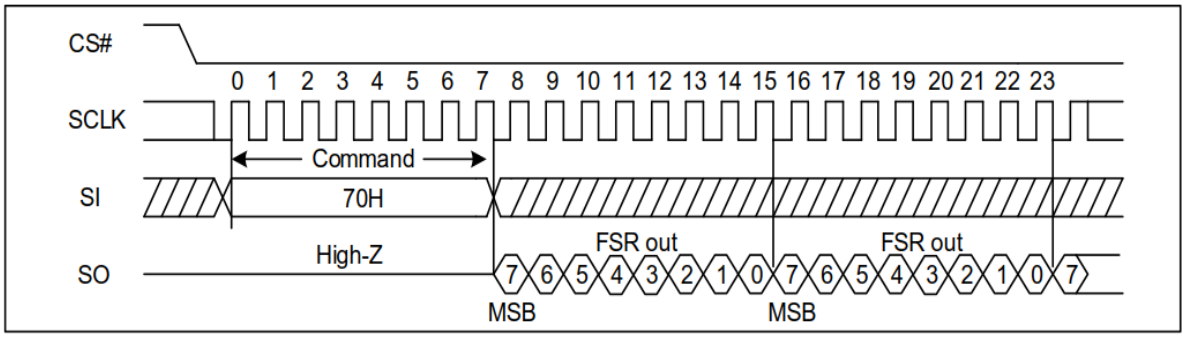


Figure 14a Read Flag Status Register Sequence Diagram (SPI)

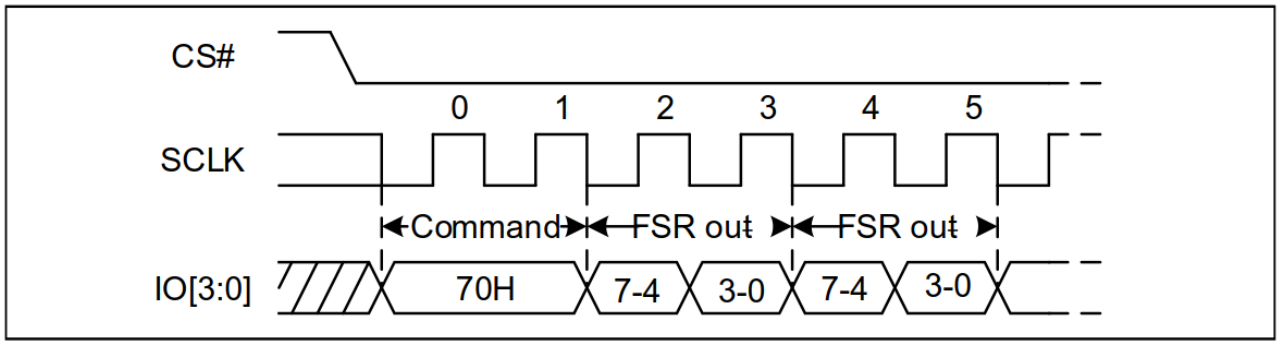


Figure 14b Read Flag Status Register Sequence Diagram (QPI)

8.2.11. Clear Flag Status Register (71H)

The Clear Flags Status Register command resets the content of Flag status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be not accepted when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

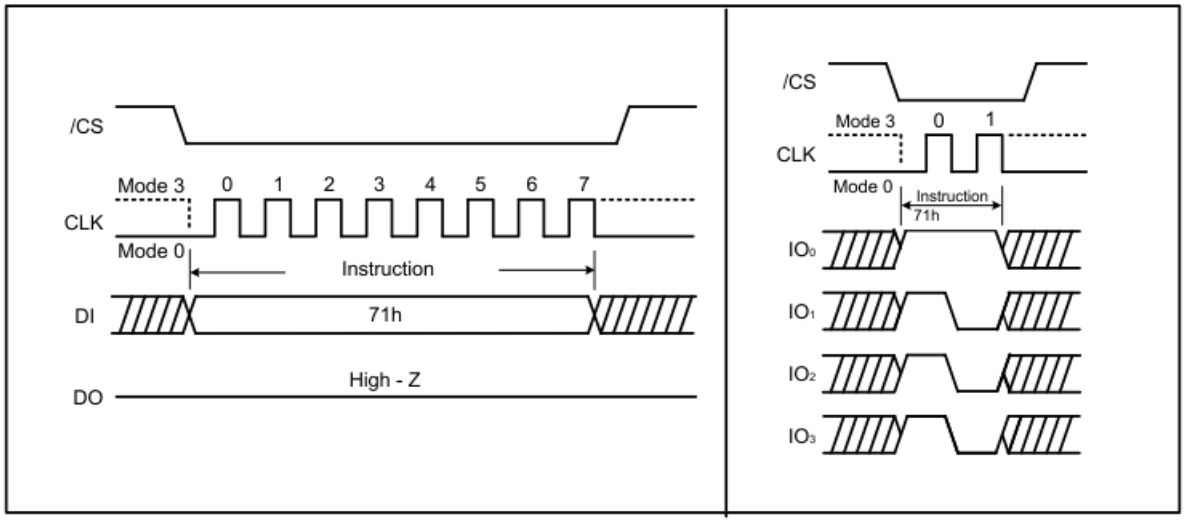


Figure 15 Clear Flag Status Register Sequence Diagram (SPI&QPI)

8.2.12. Read Configuration Register (B5H)

The Read Configuration Register command is for reading the Nonvolatile/Volatile Configuration Registers. The Configuration Register bits are then shifted out on SO, each bit is shifted out on the falling edge of SCLK. Read Nonvolatile/Volatile Configuration Register command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

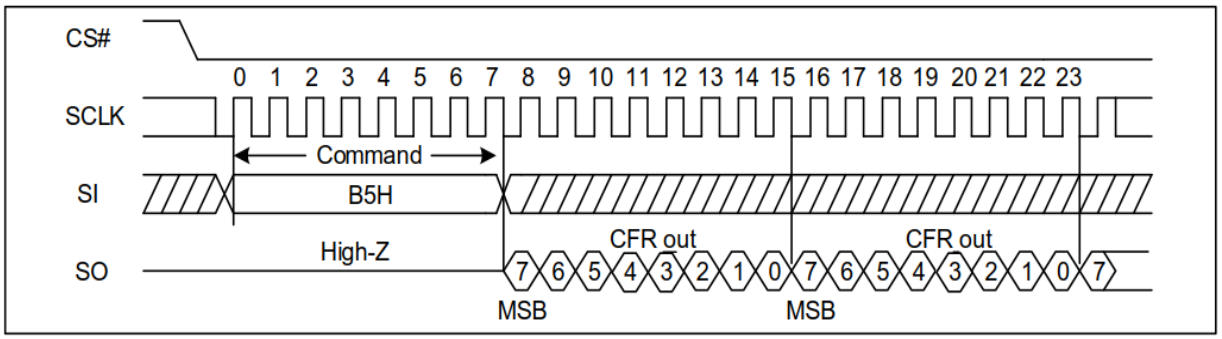


Figure 16a Read Configuration Registers Sequence Diagram (SPI)

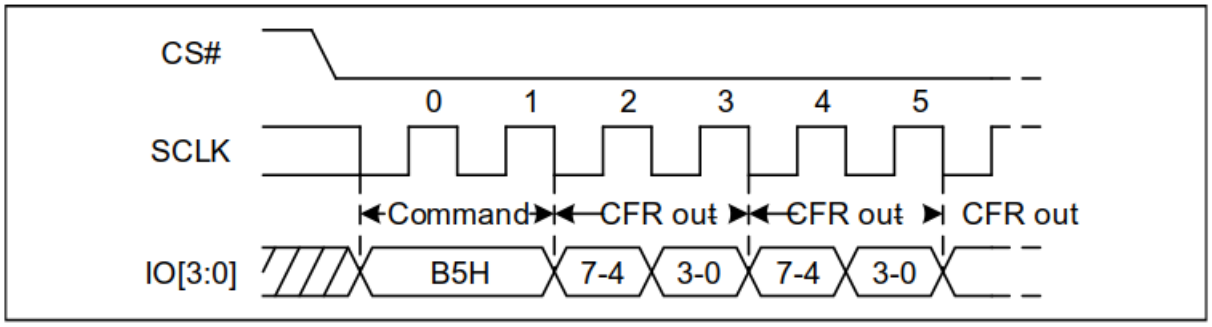


Figure 16b Read Configuration Registers Sequence Diagram (QPI)

8.2.13. **Read Extended Address Register (C8H)**

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code "C8h" into the DI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 17.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

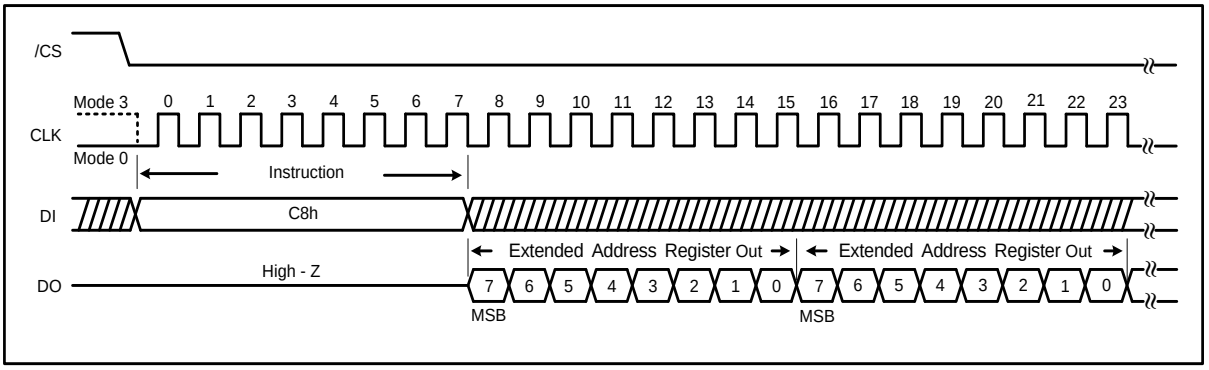


Figure 17a Read Extended Address Register Sequence Diagram (SPI)

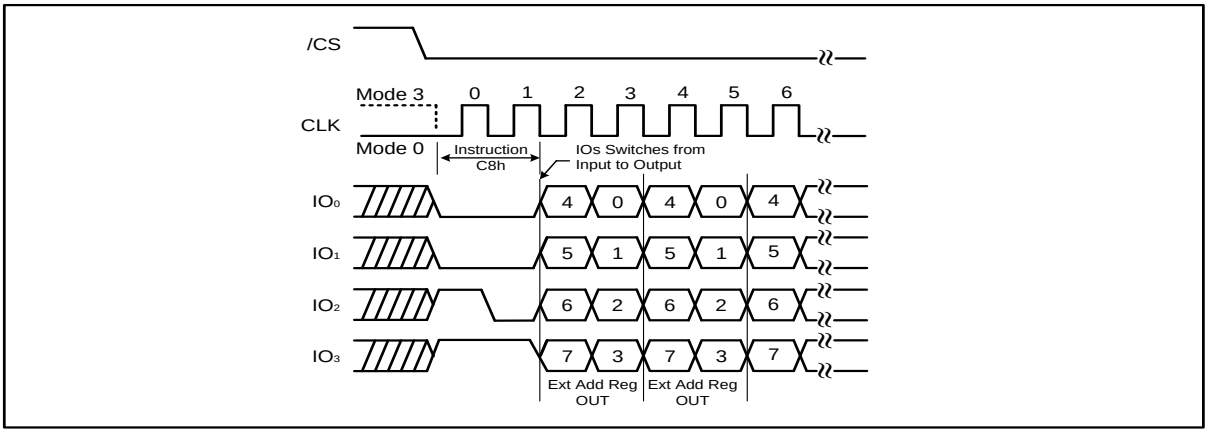


Figure 17b Read Extended Address Register Sequence Diagram (QPI)

8.2.14. **Read Data (03h/13h)**

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 18. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

The Read Data with 4-Byte Address instruction(13h) is similar to the Read Data instruction(03h). Instead of 24- bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

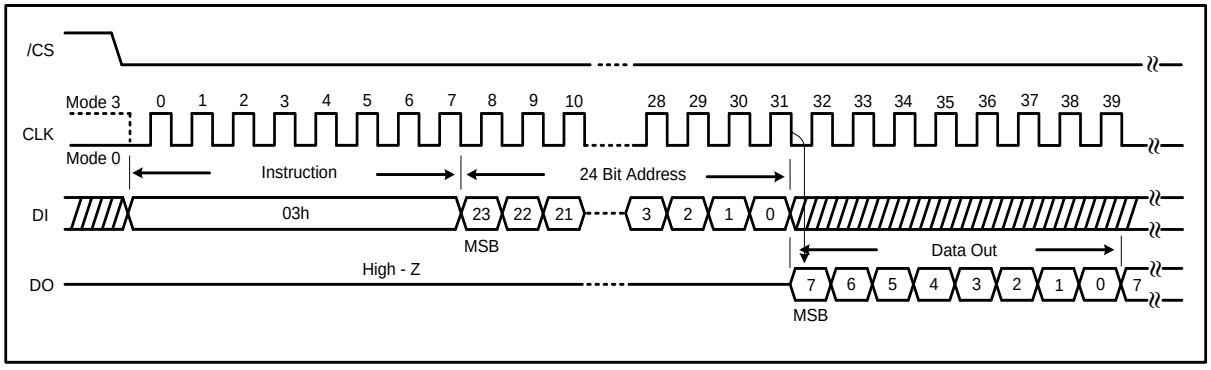


Figure 18. Read Data Instruction (SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit

8.2.15. **Fast Read (0Bh/0Ch)**

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of Fc1 (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 19. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

The Fast Read with 4-Byte Address instruction(0Ch) is similar to the Fast Read instruction(0Bh) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

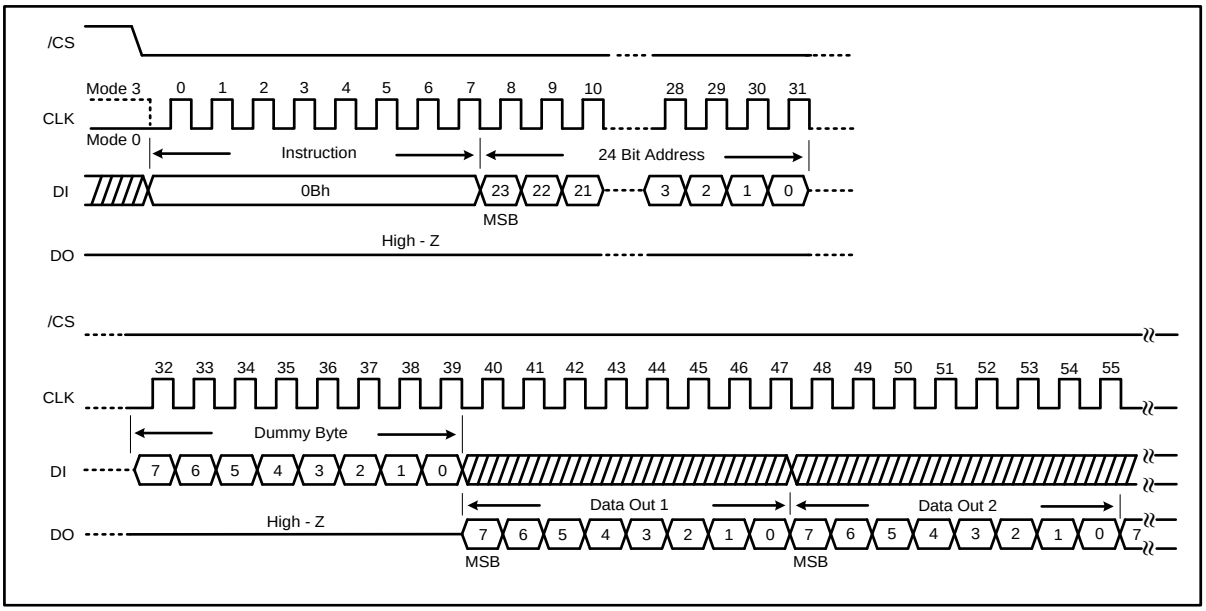


Figure 19a. Fast Read Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.16. **Fast Read (0Bh/0Ch) in QPI Mode**

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks will be set by DC bits in configuration register to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. The number of dummy clocks can be configured as either 6/8/10/12/14/16 (default = 10 upon power up or after a Reset instruction).

The Fast Read with 4-Byte Address instruction(0Ch) is similar to the Fast Read instruction(0Bh) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

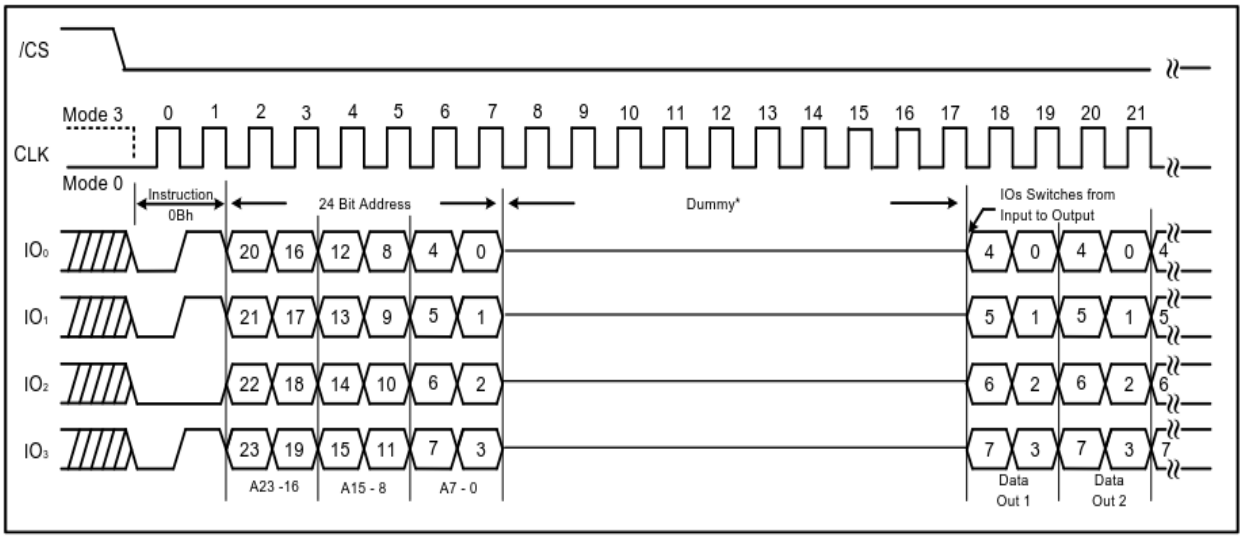


Figure 19b. Fast Read Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.17. **Fast Read Dual Output (3Bh)**

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 20. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

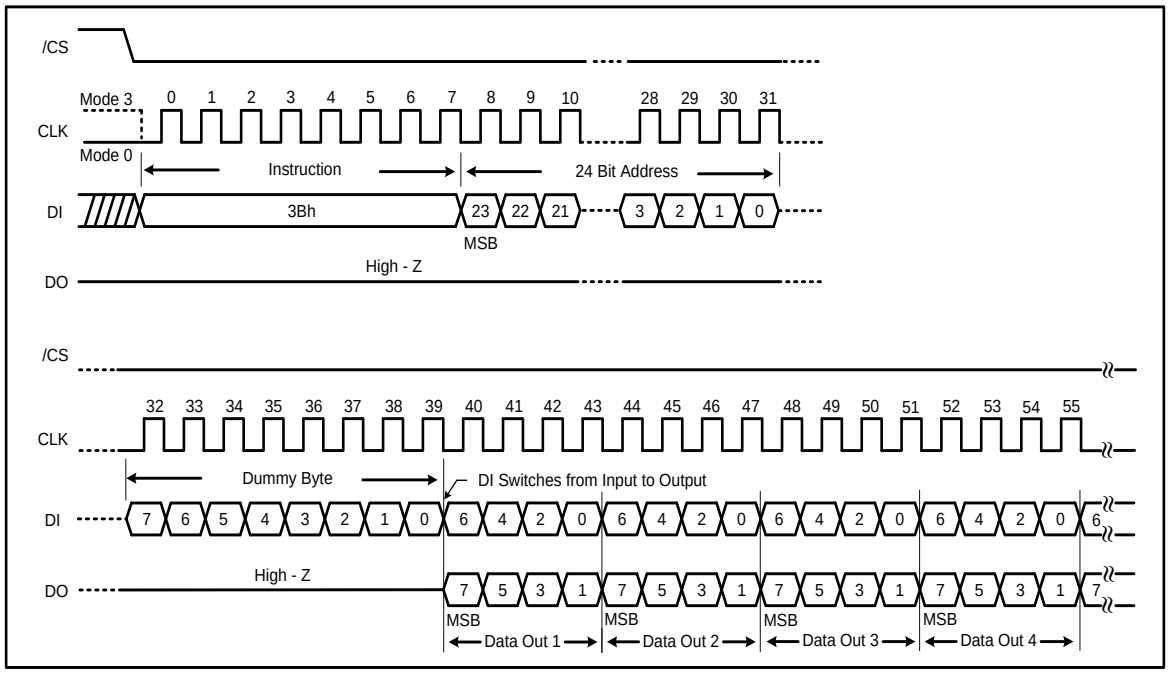


Figure 20. Fast Read Dual Output Instruction (SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.18. **Fast Read Quad Output (6Bh/6Ch)**

The Fast Read Quad Output (6Bh) instruction is similar to the standard Fast Read(0Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of Fc1 (see AC Electrical Characteristics). This is accomplished by adding 8 “dummy” clocks after the 24-bit address as shown in Figure 21. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

The Fast Read Quad Output with 4-Byte Address instruction(6Ch) is similar to the Fast Read Quad Output instruction(6Bh) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

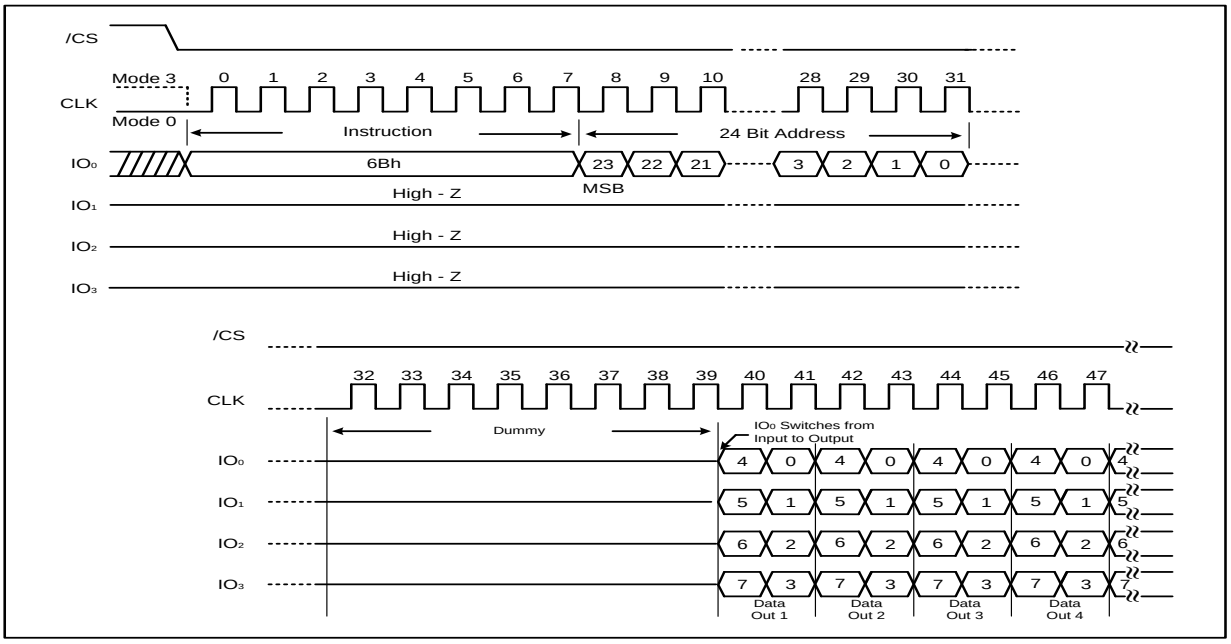


Figure 21. Fast Read Quad Output Instruction (SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.19. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications. The Fast Read Quad I/O (BBh) instruction address and data bits are input and output through two pins IO_0, IO_1, and 8 dummy clocks are required in SPI mode prior to the data output.

The number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10). The "Continuous Read Mode" bits M7-0 are counted as dummy clocks.

8.2.20. Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 22a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normaloperation.

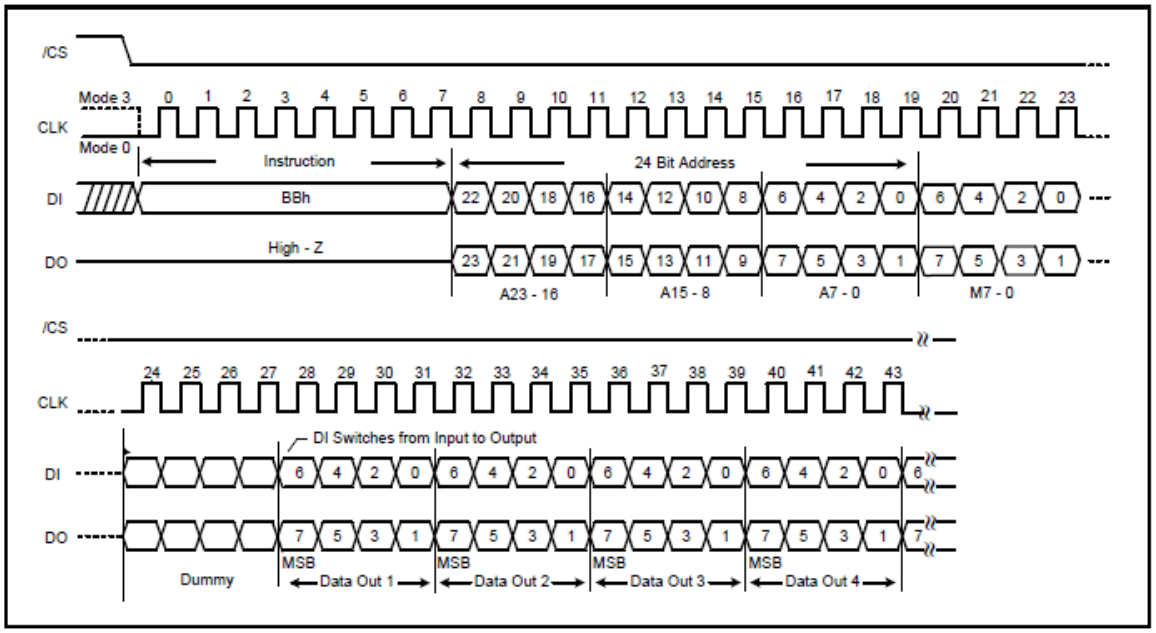


Figure 22a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

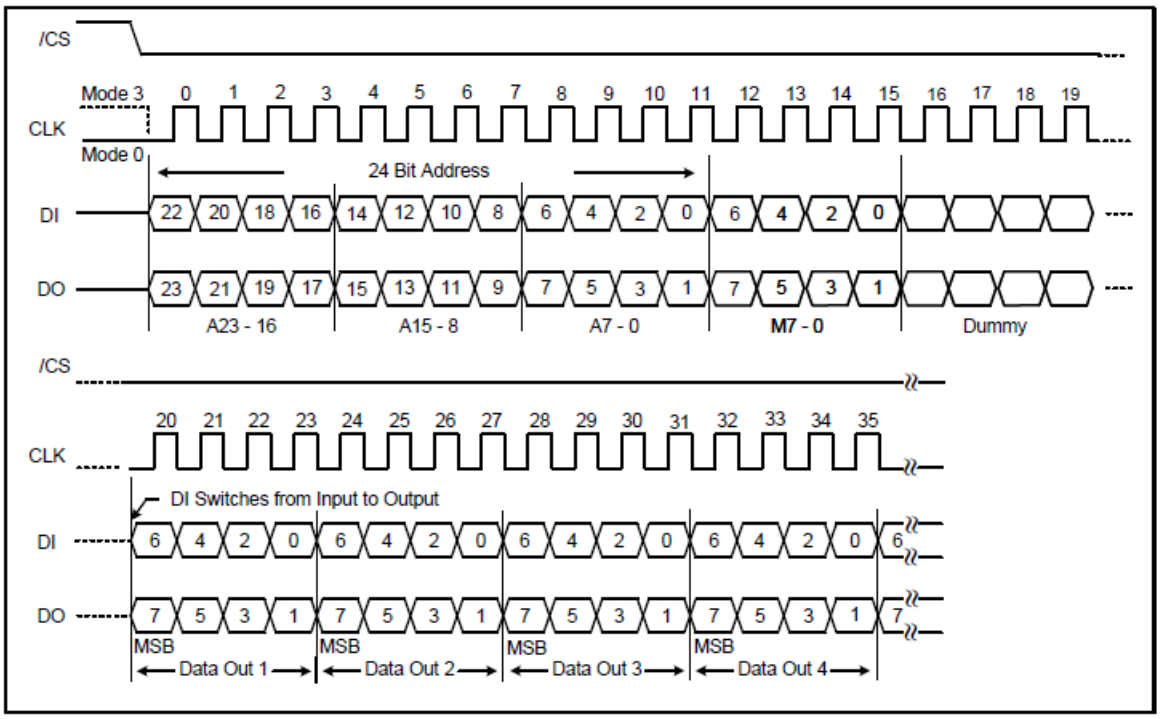


Figure 22b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.21. Fast Read Quad I/O (EBh/ECh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and several Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

The number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10). The “Continuous Read Mode” bits M7-0 are counted as dummy clocks.

The Fast Read Quad I/O with 4-Byte Address instruction(ECh) is similar to the Fast Read Quad I/O(EBh) instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

8.2.22. Fast Read Quad I/O with “Continuous Read Mode”

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 23a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 23b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

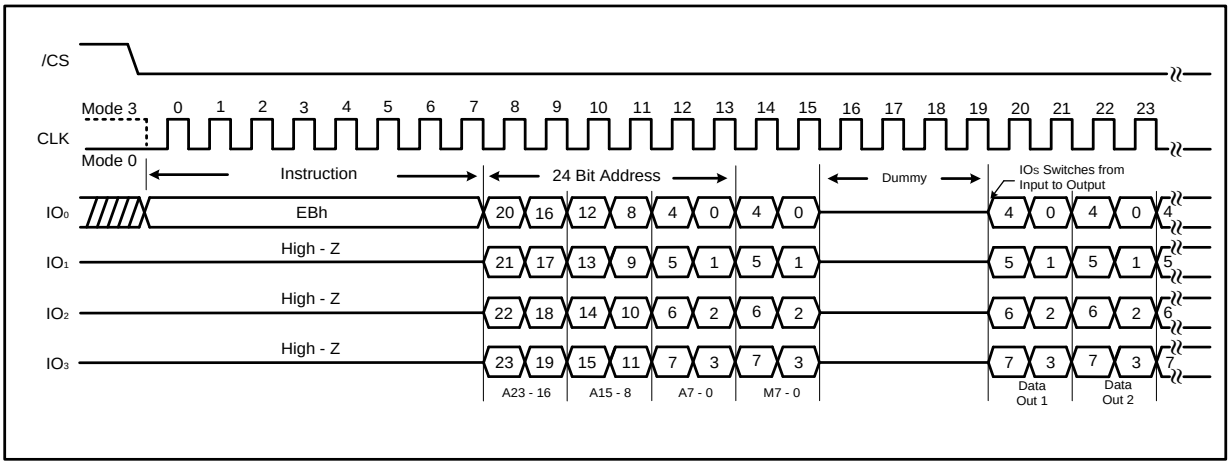


Figure 23a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

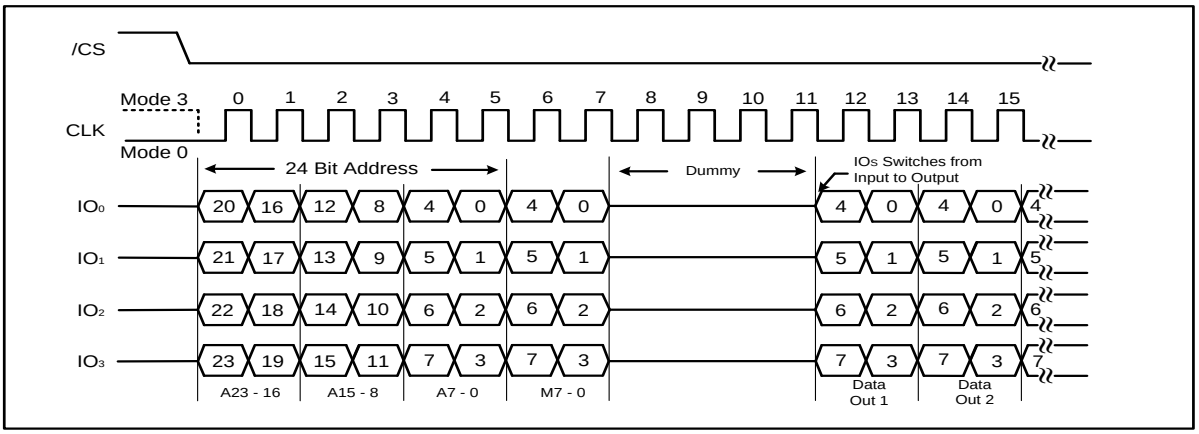


Figure 23b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.23. Fast Read Quad I/O with "16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section "Set Burst with Wrap" for detail descriptions.

8.2.24. Fast Read Quad I/O (EBh/ECh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 23c. When QPI mode is enabled, The number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10 upon power up or after a Reset instruction). In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

The Fast Read Quad I/O with 4-Byte Address instruction(ECh) is similar to the Fast Read Quad I/O instruction(EBh) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

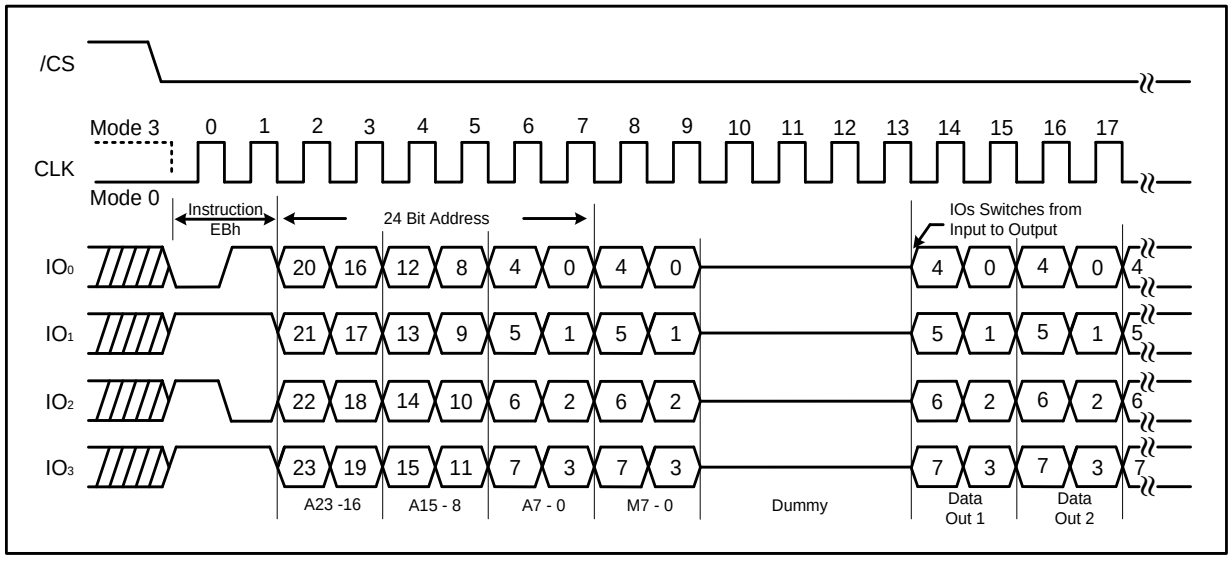


Figure 23c. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.25. Fast Read Quad I/O with "16/32/64-Byte Wrap Around" in QPI mode

The Fast Read Quad I/O instruction can also be used with wrap around. Please refer to Set Read Parameters (C0h).

8.2.26. Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" and "DTR Read Quad I/O" instructions to access a fixed length of 16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Figure 24. Wrap bit W7 and the lower nibble W3-0 are not used.

Table16. Wrap Bit Definition

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	16-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" and "DTR Read Quad I/O" instructions will use the W6-4 setting to access the 16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, The Wrap Length set by W6-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0h)" instruction. Refer to section "Set Read Parameters" for details.

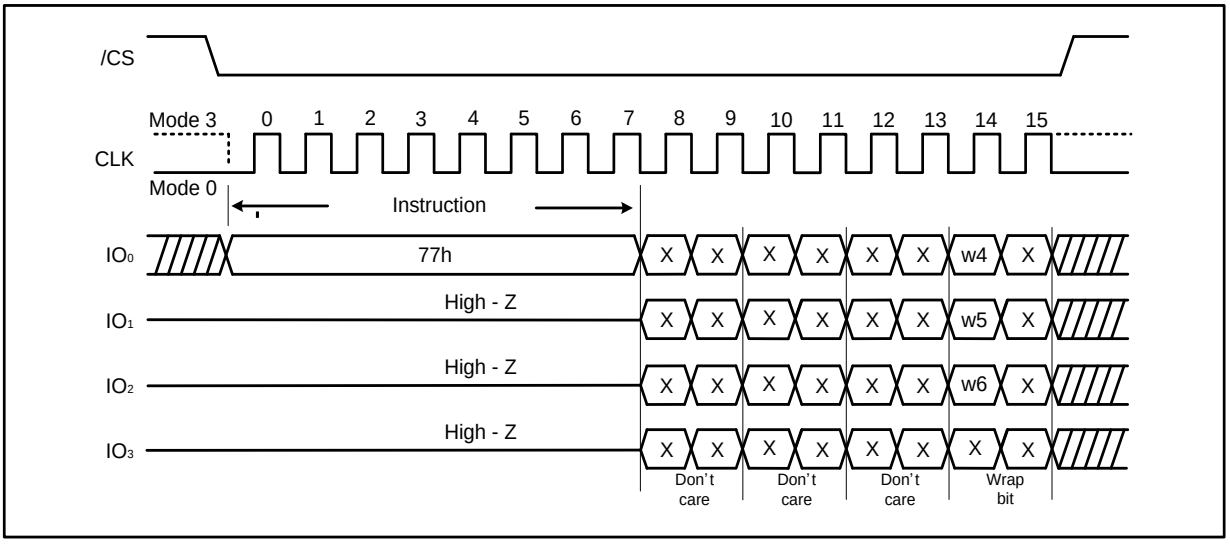


Figure 24. Set Burst with Wrap Instruction (SPI Mode only)

8.2.27. DTR Read Quad I/O (EDh/EEh)

The DTR Read Quad I/O instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of Status Register must be set to "1" before sending the DTR Read Quad I/O instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of CLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single DTR Read Quad I/O instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

The number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10). "Continuous Read Mode" bits M7-0 are counted as dummy clocks.

The DTR Read Quad I/O with 4-Byte Address instruction(EEh) is similar to the DTR Read Quad I/O instruction(EDh) except that it requires 32-bit address instead of 24-bit address. No matter that the device is operating in 3-Byte Address Mode or 4-byte Address Mode, The DTR Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

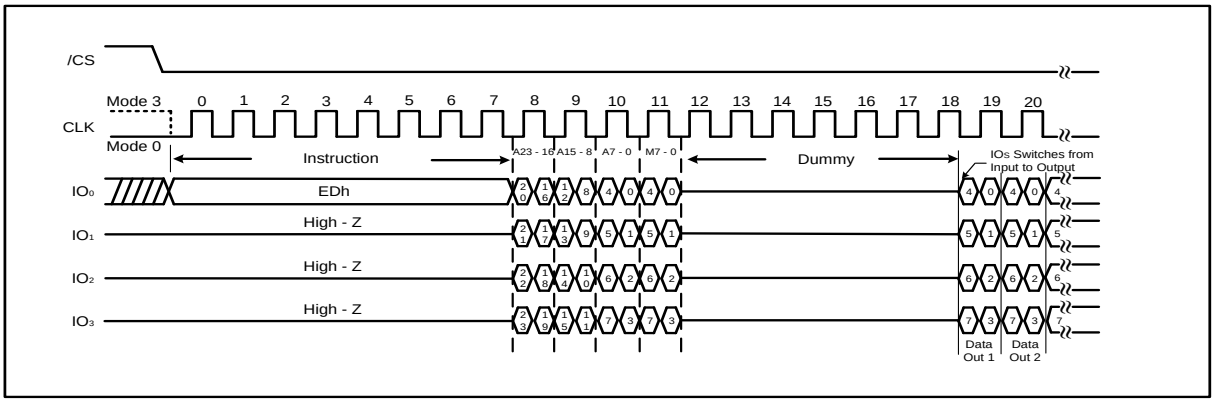


Figure 25a. DTR Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit

8.2.28. DTR Read Quad I/O with "Continuous Read Mode"

The DTR Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 25a. The upper nibble of the (M7-4) controls the length of the next DTR Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EDh instruction code, as shown in Figure 25b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

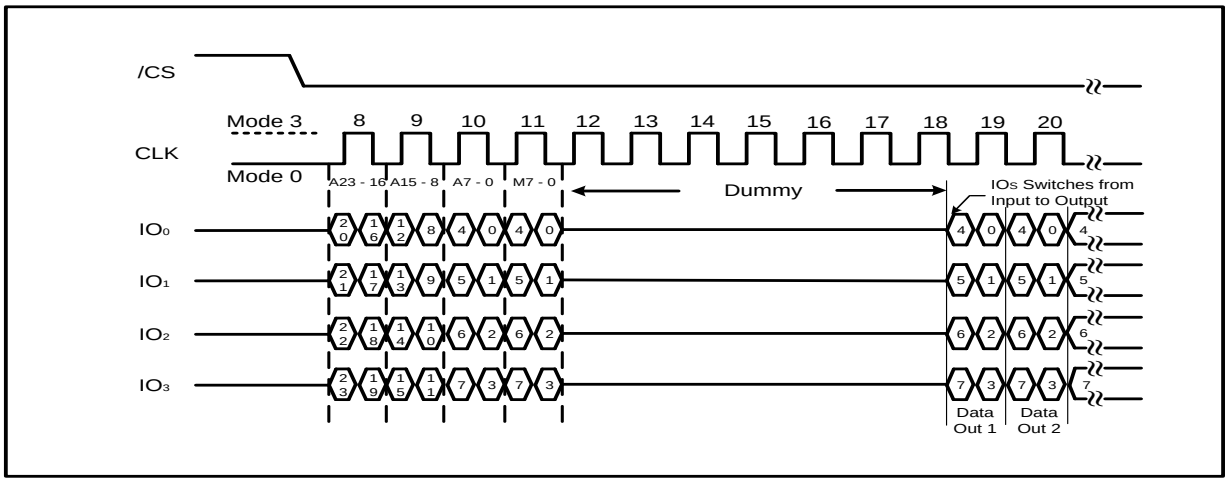


Figure 25b. DTR Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.29. DTR Read Quad I/O with "16/32/64-Byte Wrap Around" in Standard SPI mode

The DTR Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section "Set Burst with Wrap" for detail descriptions.

8.2.30. DTR Read Quad I/O (EDh/EEh) in QPI Mode

The DTR Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 25c.

The number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10). "Continuous Read Mode" bits M7-0 are also considered as dummy clocks.

In QPI mode, In the default setting, the data output will follow the Continuous Read Mode bits immediately.

The DTR Read Quad I/O with 4-Byte Address(EEh) instruction is similar to the DTR Read Quad I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter that the device is operating in 3-Byte Address Mode or 4-byte Address Mode, The DTR Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

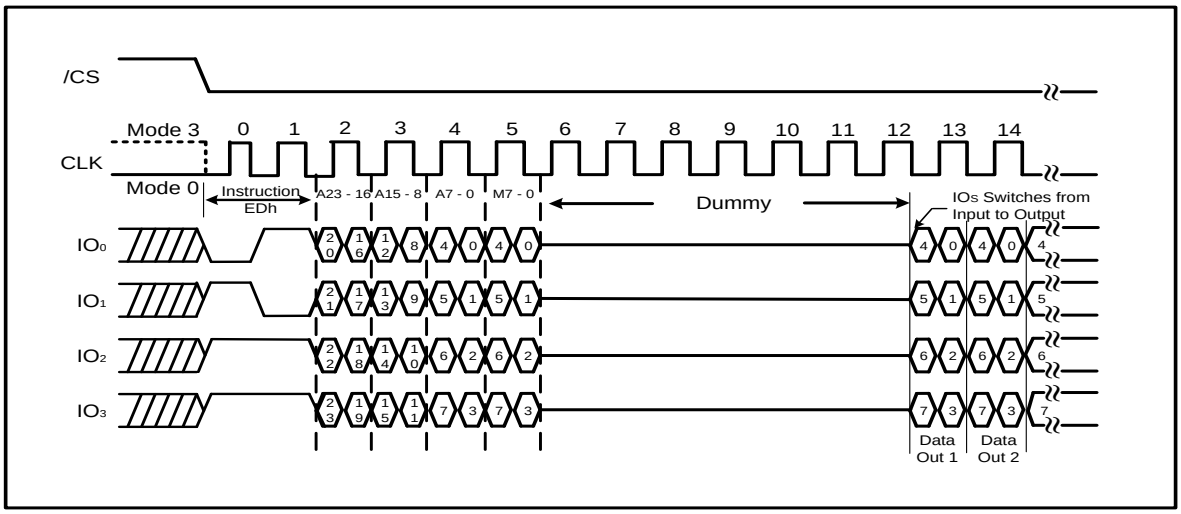


Figure25c. DTR Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.31. **DTR Read Quad I/O with "16/32/64-Byte Wrap Around" in QPI mode**

The DTR Read Quad I/O instruction can also be used with wrap around. Please refer to Set Read Parameters (C0h).

8.2.32. **Page Program (02h/12h)**

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 26.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

The Page Program with 4-Byte Address instruction(12h) is similar to the Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

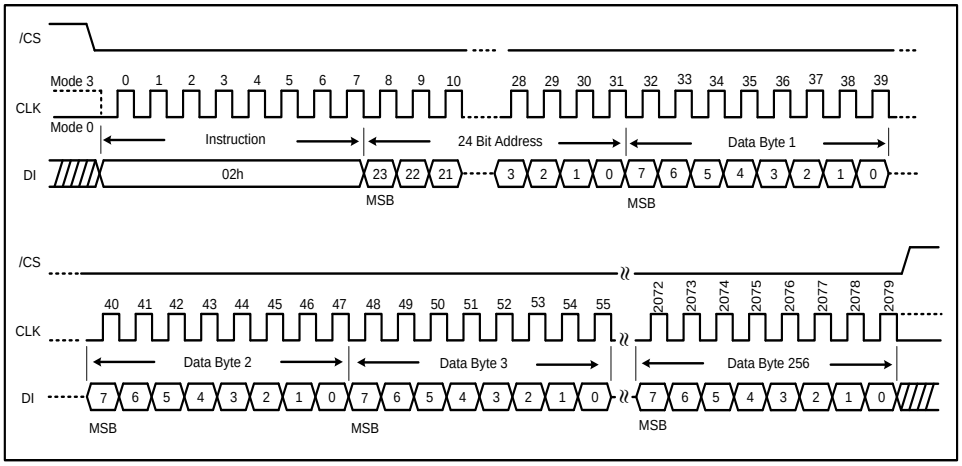


Figure 26a. Page Program Instruction (SPI Mode)

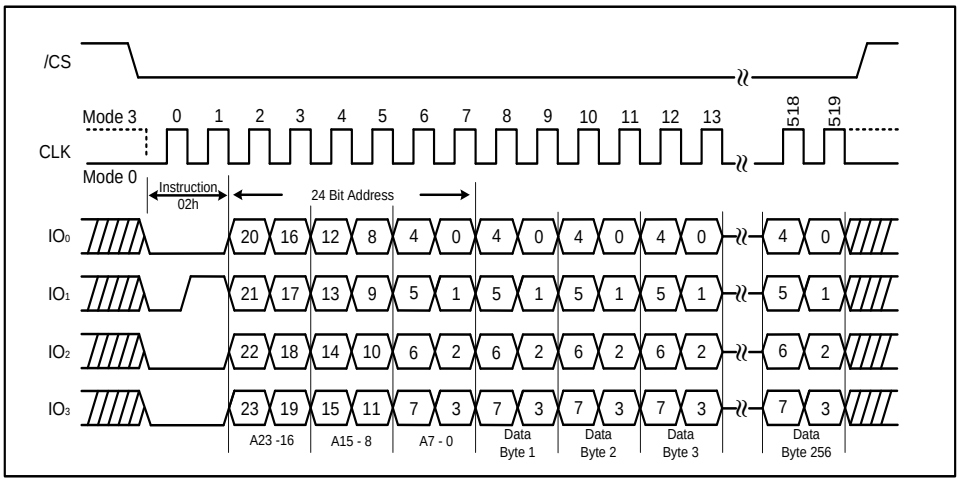


Figure 26b. Page Program Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.33. Quad Input Page Program (32h/34h)

The Quad Input Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Input Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Input Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Input Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Input Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Input Page Program are identical to standard Page Program. The Quad Input Page Program instruction sequence is shown in Figure 27.

The Quad Input Page Program with 4-Byte Address instruction(34h) is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

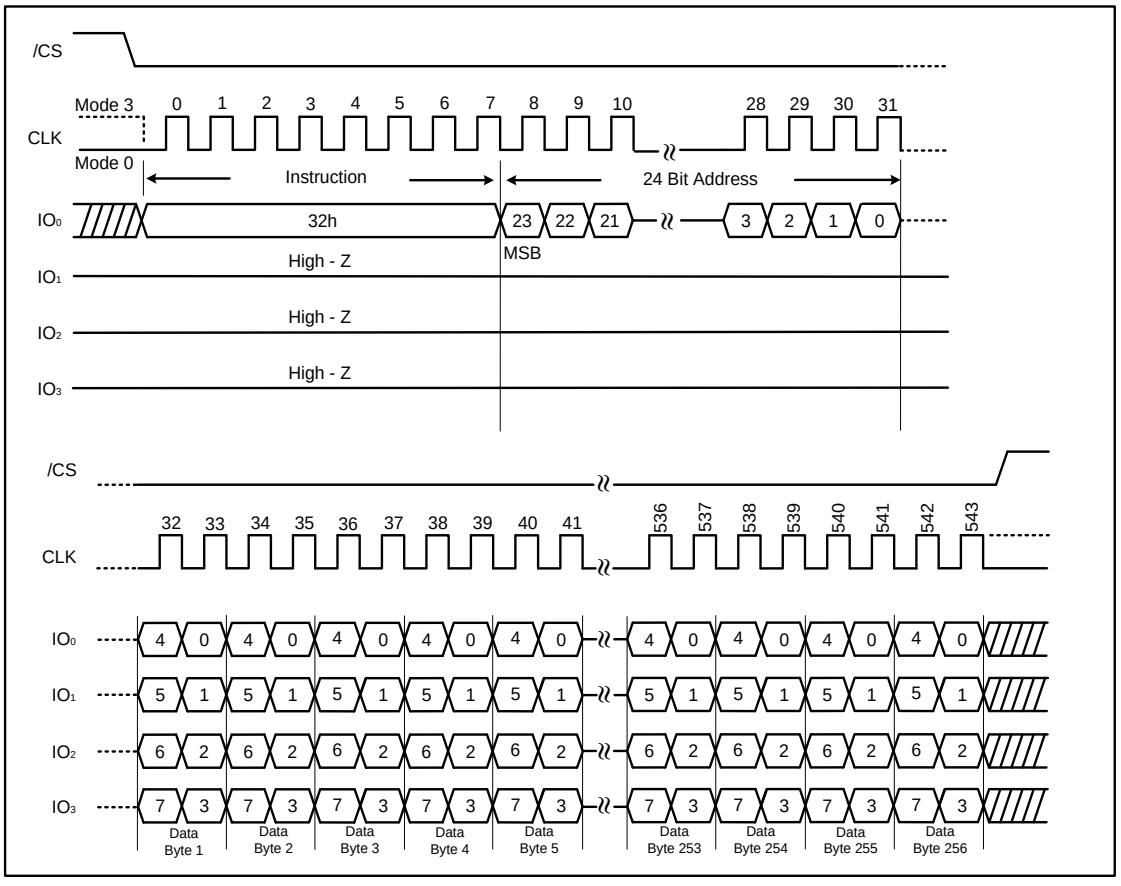


Figure 27. Quad Input Page Program Instruction (SPI Mode only)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.34. Extend Quad Page Program (C2H/3EH)

The Extend Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend quad Page Program command is entered by driving CS# Low, followed by the command code (C2H/3EH), three or four address Bytes and at least one data Byte on IO pins.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Extend Quad Page Program (EPP) command is not executed.

As soon as CS# is driven high, the self-timed Extend Quad Page Program cycle (whose duration is tPP) is initiated. While the Extend Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

An Extend Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1 and BP0) is not executed.

The Extend Quad Page Program with 4-Byte Address instruction(3Eh) is similar to the Extend Quad Page Program instruction(C2h) except that it requires 32-bit address instead of 24-bit address. The Extend Quad Page Program with 4-Byte Address can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program with 4-Byte Address instruction since the inherent page program time is much greater than the time it take to clock-in the data. To use Quad Page Program with 4-Byte Address the Quad Enable (QE) bit must be set to 1. The Quad Page Program with 4-Byte Address instruction sequence is shown in Figure 28.

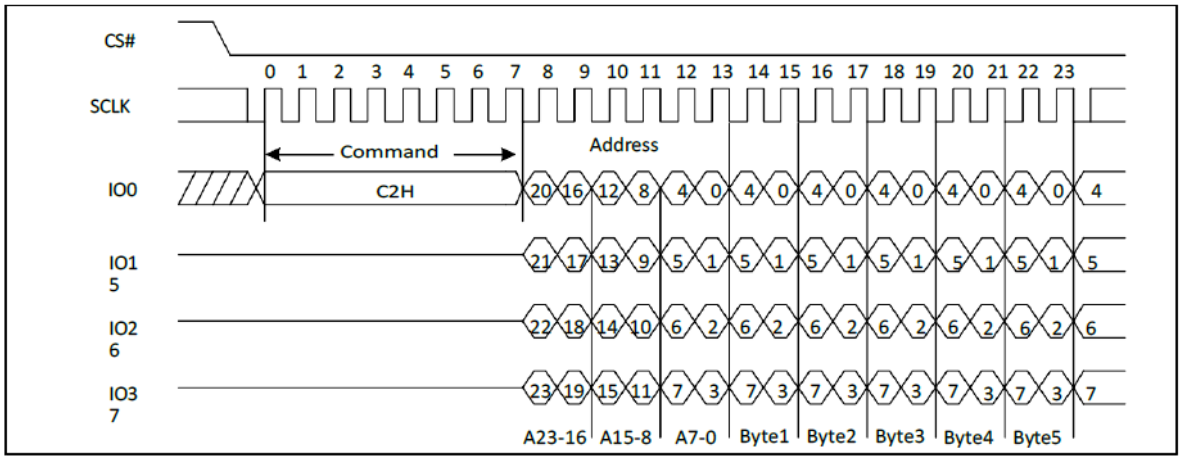


Figure 28 Extend Quad Page Program Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.35. Sector Erase (20h/21h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 29a & 29b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

The Sector Erase with 4-Byte Address instruction(21h) is similar to the Sector Erase instruction(20h) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

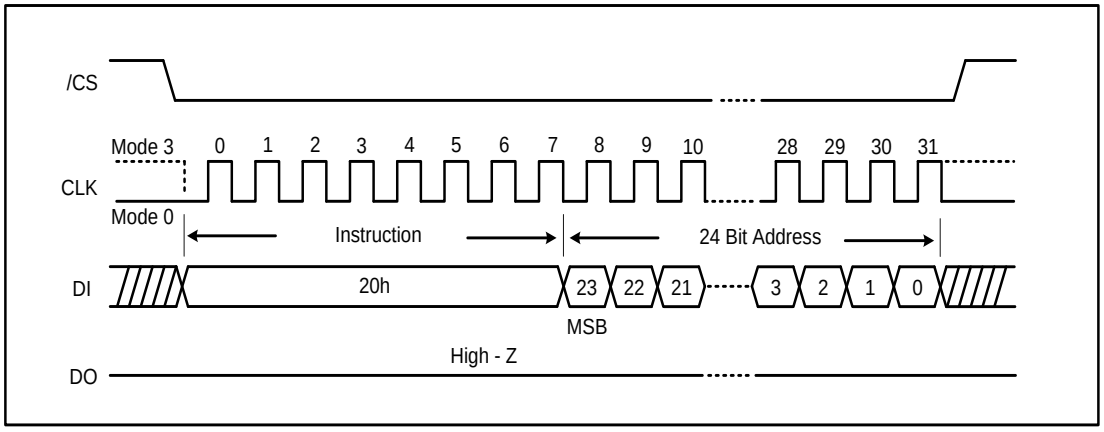


Figure 29a. Sector Erase Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

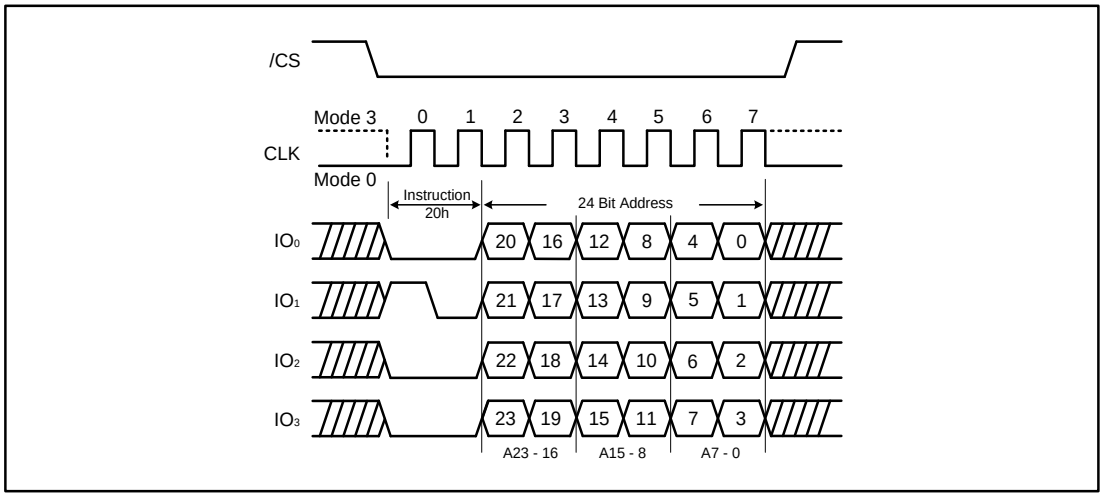


Figure 29b. Sector Erase Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.36. **32KB Block Erase (52h/5Ch)**

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register

bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 30a & 30b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

The 32KB Block Erase with 4-Byte Address instruction(5Ch) is similar to the 32KB Block Erase instruction(52h) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-ByteAddress Mode or 4-byte Address Mode, the 32KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

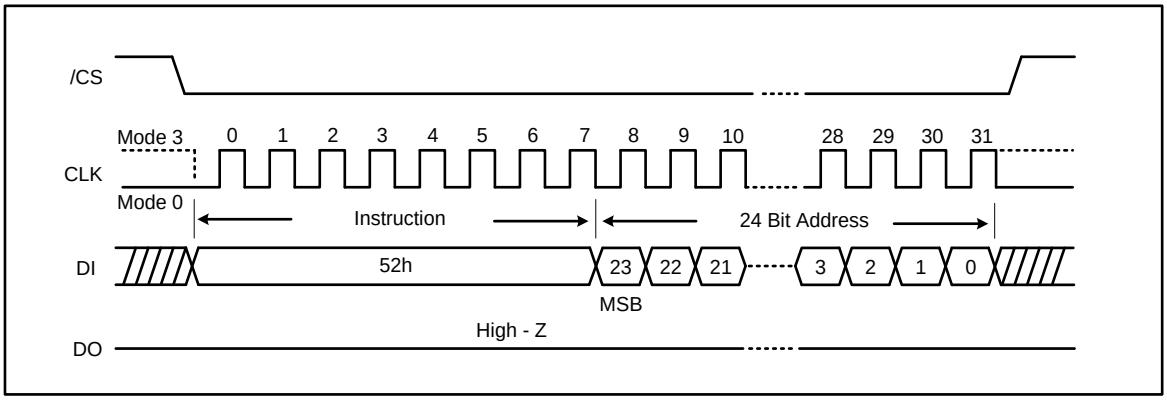


Figure 30a. 32KB Block Erase Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

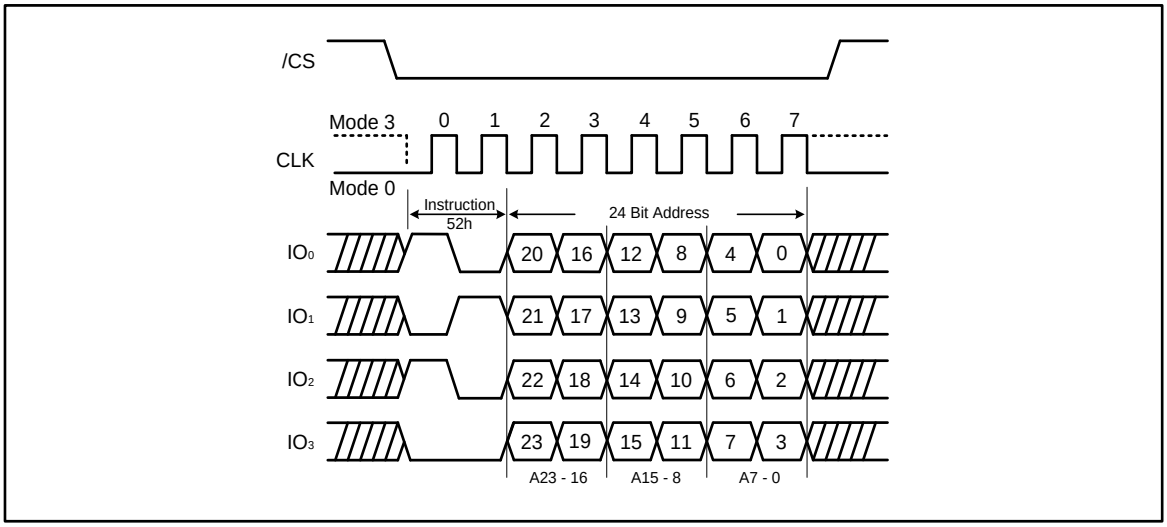


Figure 30b. 32KB Block Erase Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.37. 64KB Block Erase (D8h/DCh)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 31a & 31b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

The 64KB Block Erase with 4-Byte Address instruction(D8h) is similar to the 64KB Block Erase instruction(DCh) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-ByteAddress Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

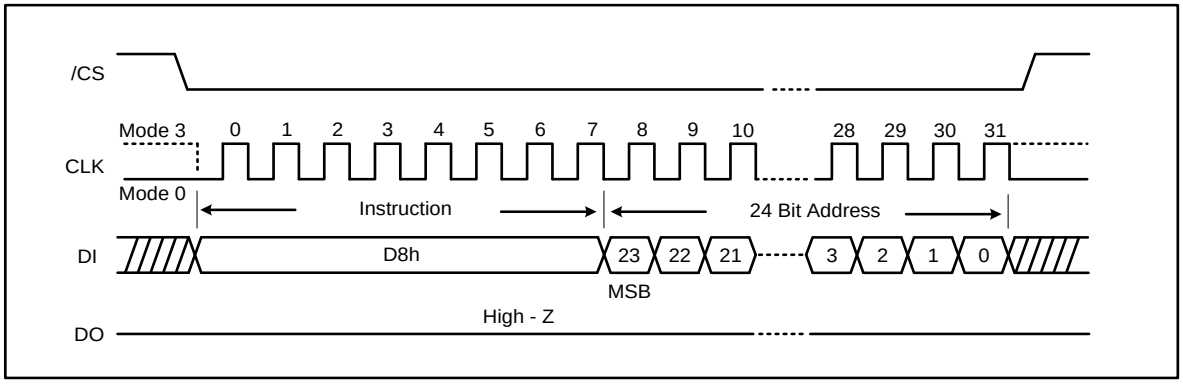


Figure 31a. 64KB Block Erase Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

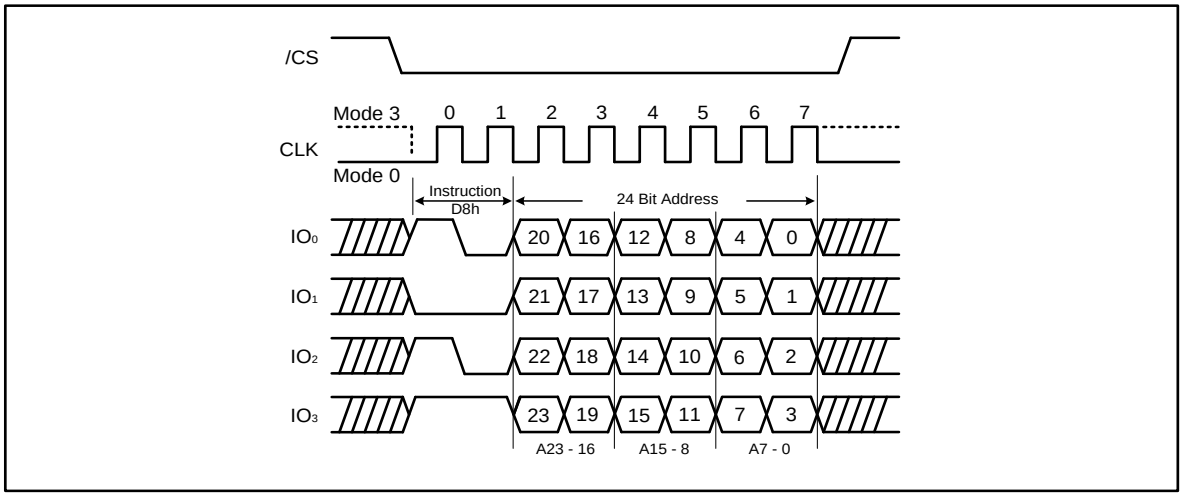


Figure 31b. 64KB Block Erase Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.38. **Chip Erase (C7h / 60h)**

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 32.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

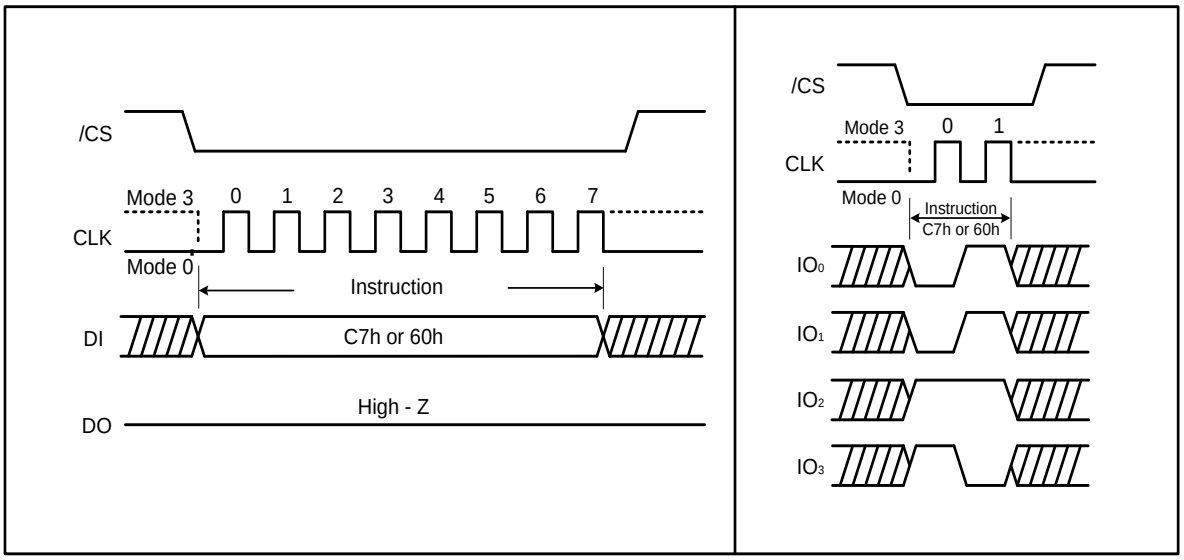


Figure 32. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

8.2.39. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 33a & 33b.

The Write Status Register(01h, 31h, 11h), Write Configuration Register(B1h), Write Password(28H) instruction and Erase instructions (20h/21h, 52h/D8h, 5Ch/DCh， C7h/60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored.

The Write Status Register(01h, 31h, 11h), Write Configuration Register(B1h), Write Password(28H) instruction and Erase instructions (20h/21h, 52h/D8h, 5Ch/DCh， C7h/60h, 44h) and Program instructions (02h/12h, 32h/34h, C2h/3Eh, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program, Quad Page Program operation or Extended Quad Page Program.

Individual/global block/sector lock/unlock instructions should not be issued when Erase/Program is Suspended.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the both SUS1 and SUS2 bits in the Status Register equal to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If at least one of SUS1/SUS2 bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

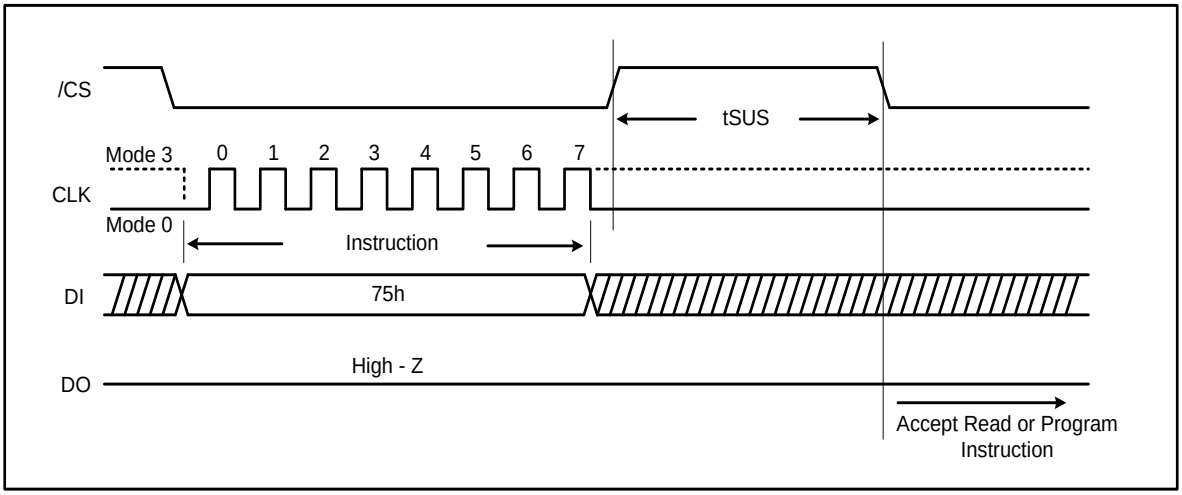


Figure 33a. Erase/Program Suspend Instruction (SPI Mode)

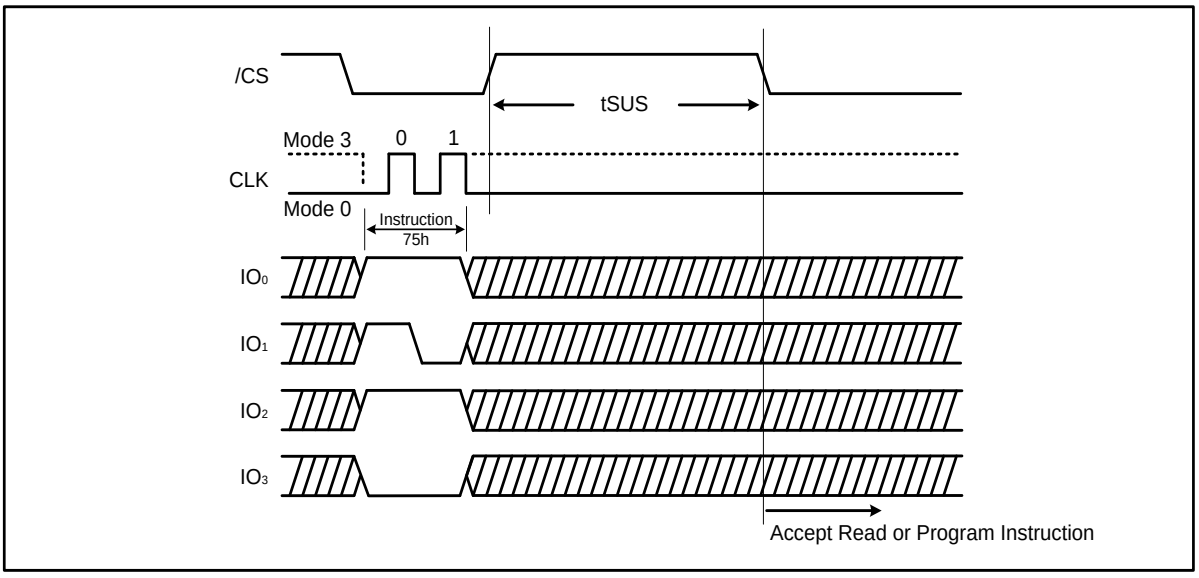


Figure 33b. Erase/Program Suspend Instruction (QPI Mode)

8.2.40. **Erase / Program Resume (7Ah)**

The Erase/Program Resume instruction "7Ah" must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction "7Ah" will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction "7Ah" will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 34a & 34b.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of "tSUS" following a previous Resume instruction.

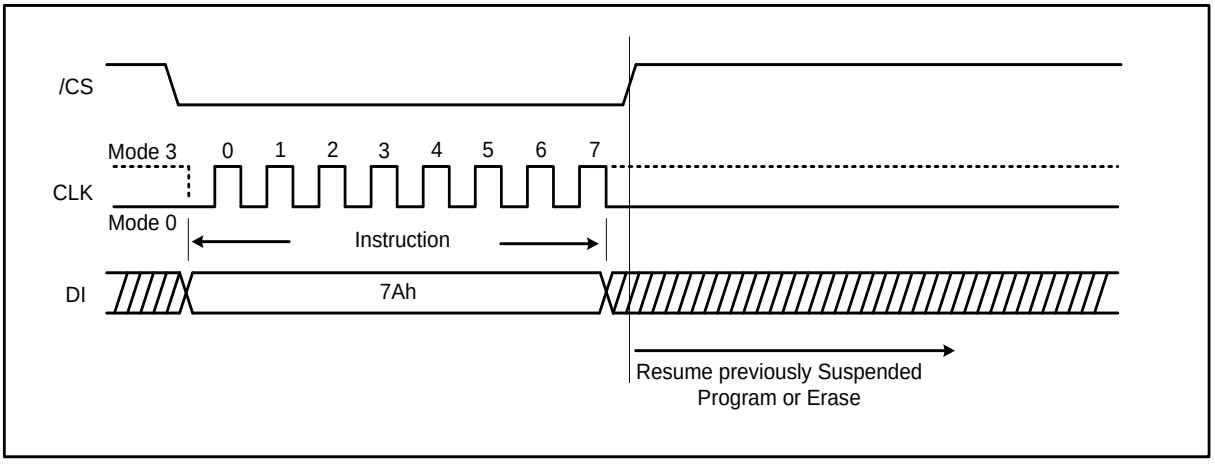


Figure 34a. Erase/Program Resume Instruction (SPI Mode)

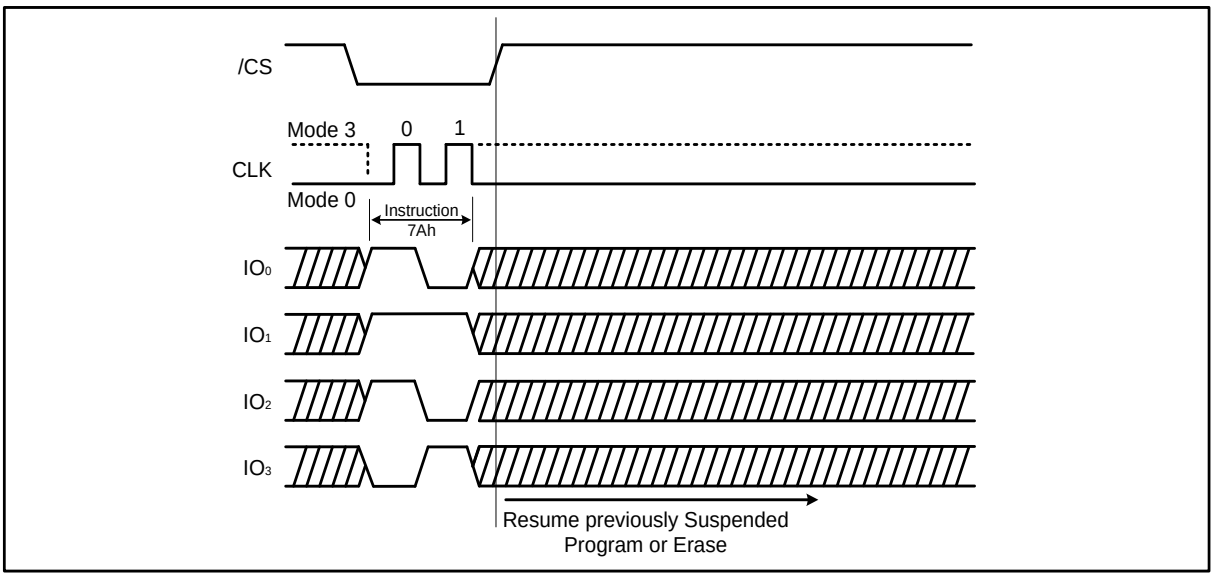


Figure 34b. Erase/Program Resume Instruction (QPI Mode)

8.2.41. **Deep Power-down (B9h)**

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 35a & 35b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power- down / Device ID (ABh) instruction, which restores the device to normal operation, and software reset(66H+99H) will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Deep Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

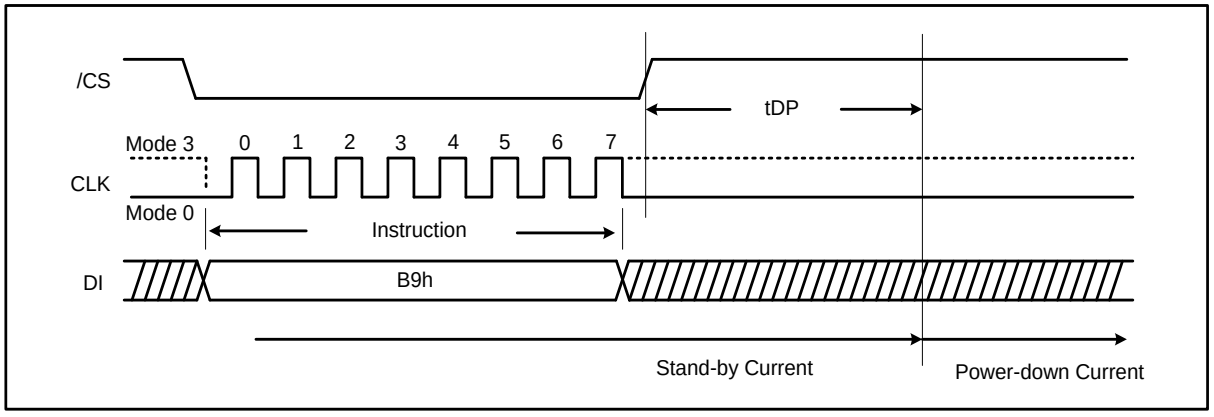


Figure 35a. Deep Power-down Instruction (SPI Mode)

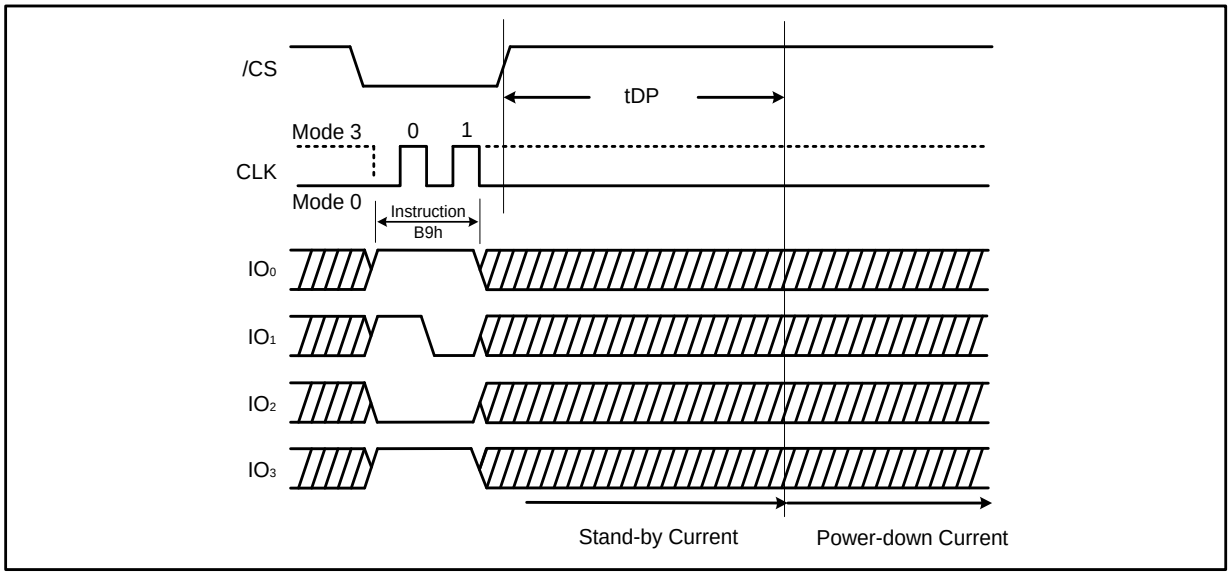


Figure 35b. Deep Power-down Instruction (QPI Mode)

8.2.42. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 36a & 36b. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the DS25Q4DN is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 36c & 36d, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power- down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

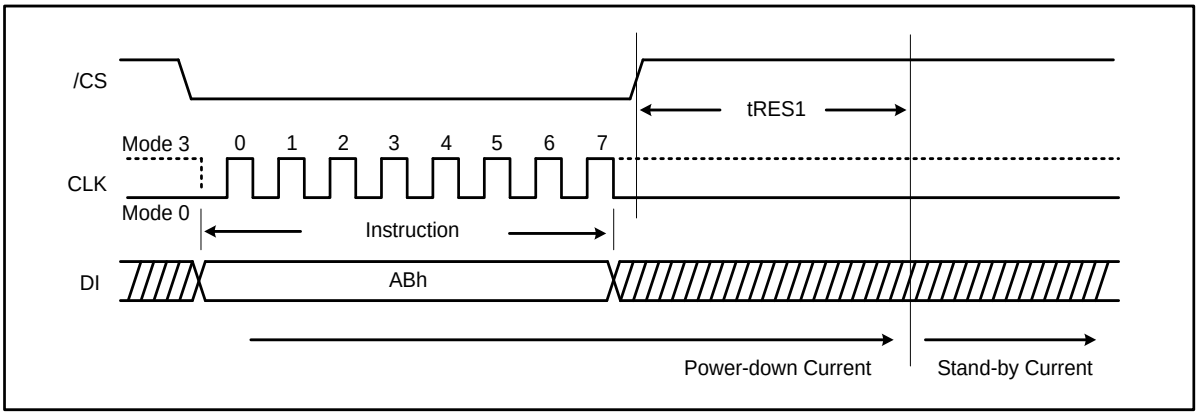


Figure 36a. Release Power-down Instruction (SPI Mode)

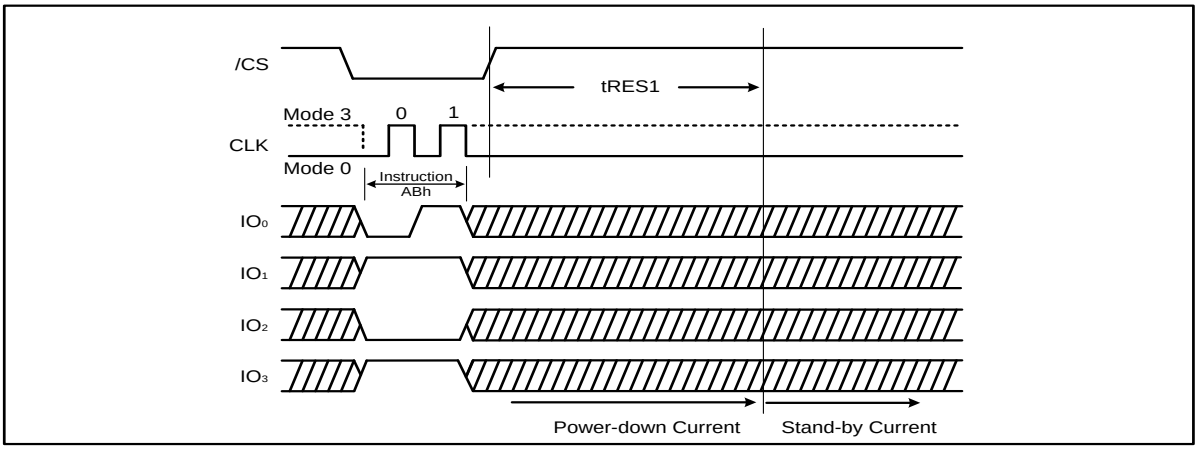


Figure 36b. Release Power-down Instruction (QPI Mode)

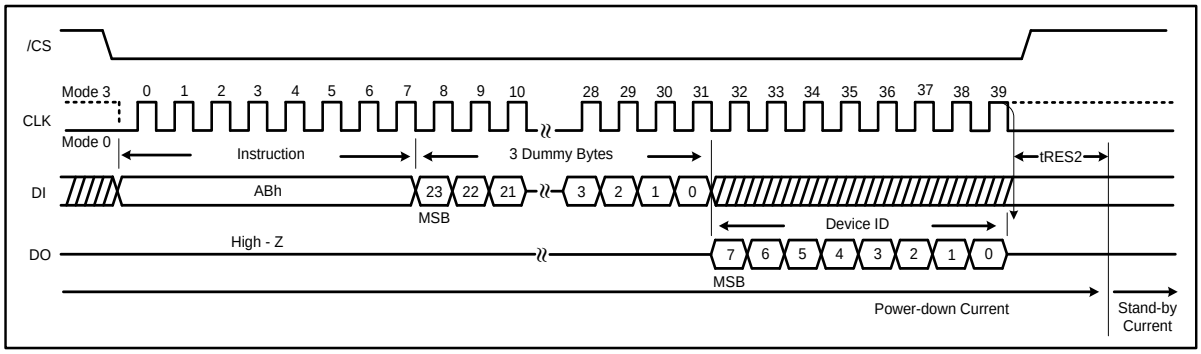


Figure 36c. Release Power-down / Device ID Instruction (SPI Mode)

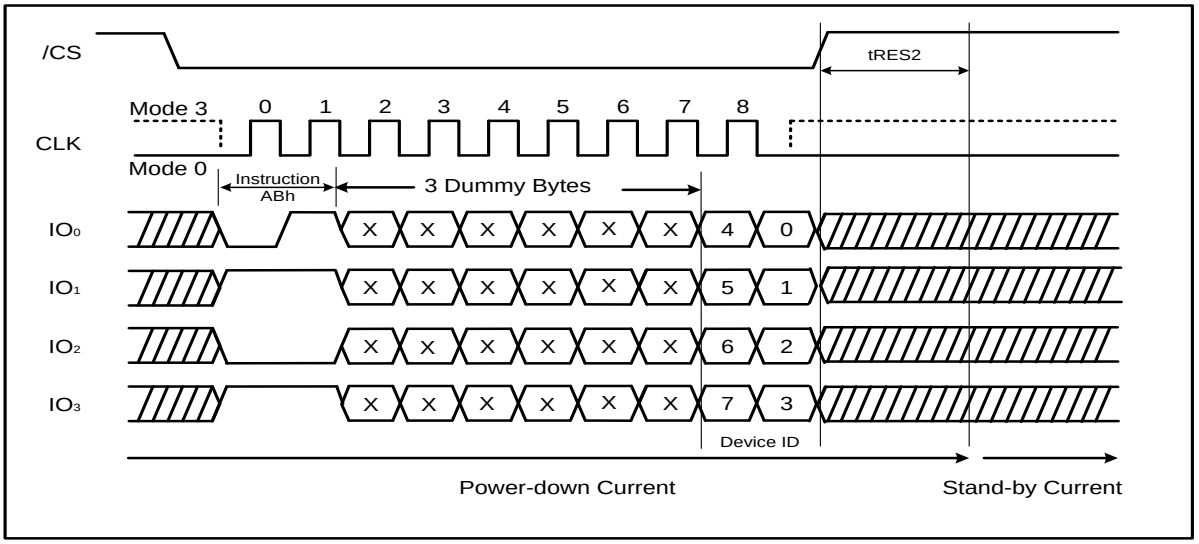


Figure 36d. Release Power-down / Device ID Instruction (QPI Mode)

8.2.43. **Read Manufacturer / Device ID (90h)**

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Dosilicon (E5h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 37. The Device ID values for the DS25Q4DN are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

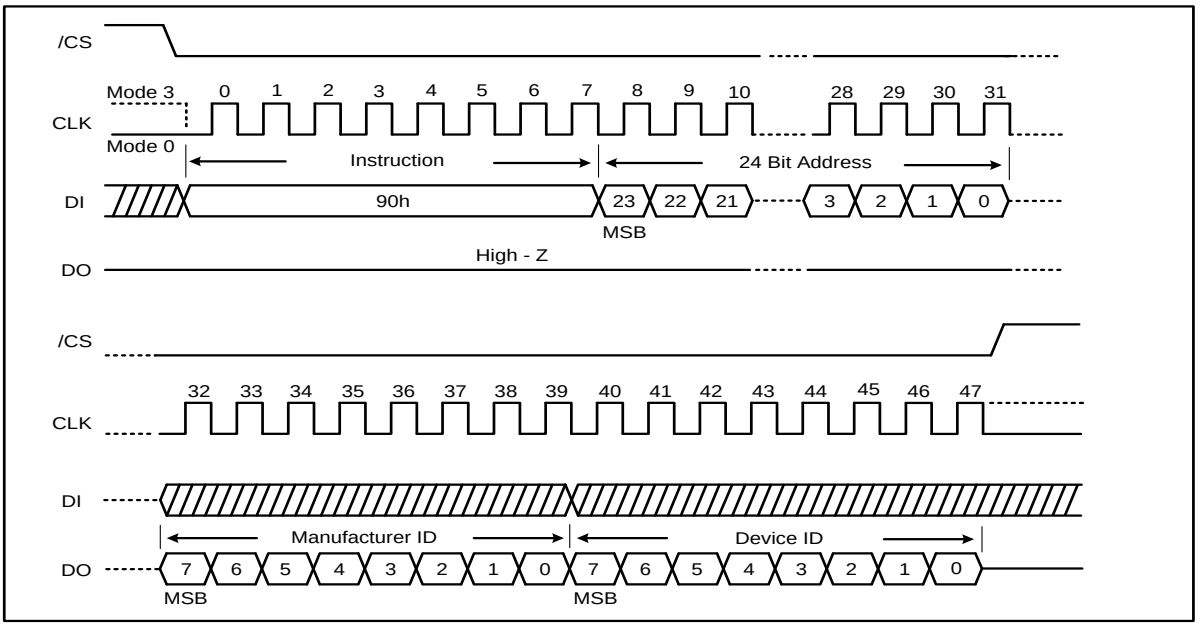


Figure 37a. Read Manufacturer / Device ID Instruction (SPI Mode)

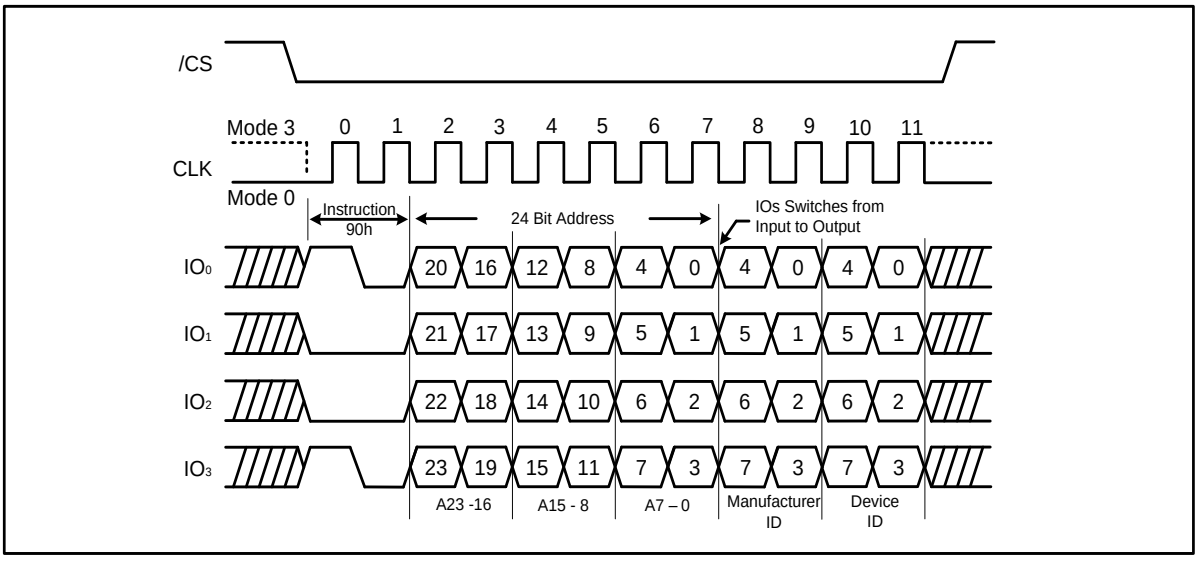


Figure 37b. Read Manufacturer / Device ID Instruction (QPI Mode)

8.2.44. Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "94h" followed by a 24-bit address (A23-A0) of 000000h and then a 8 clock dummy cycles, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Dosilicon (E5h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 38. The Device ID values for the DS25Q4DN are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

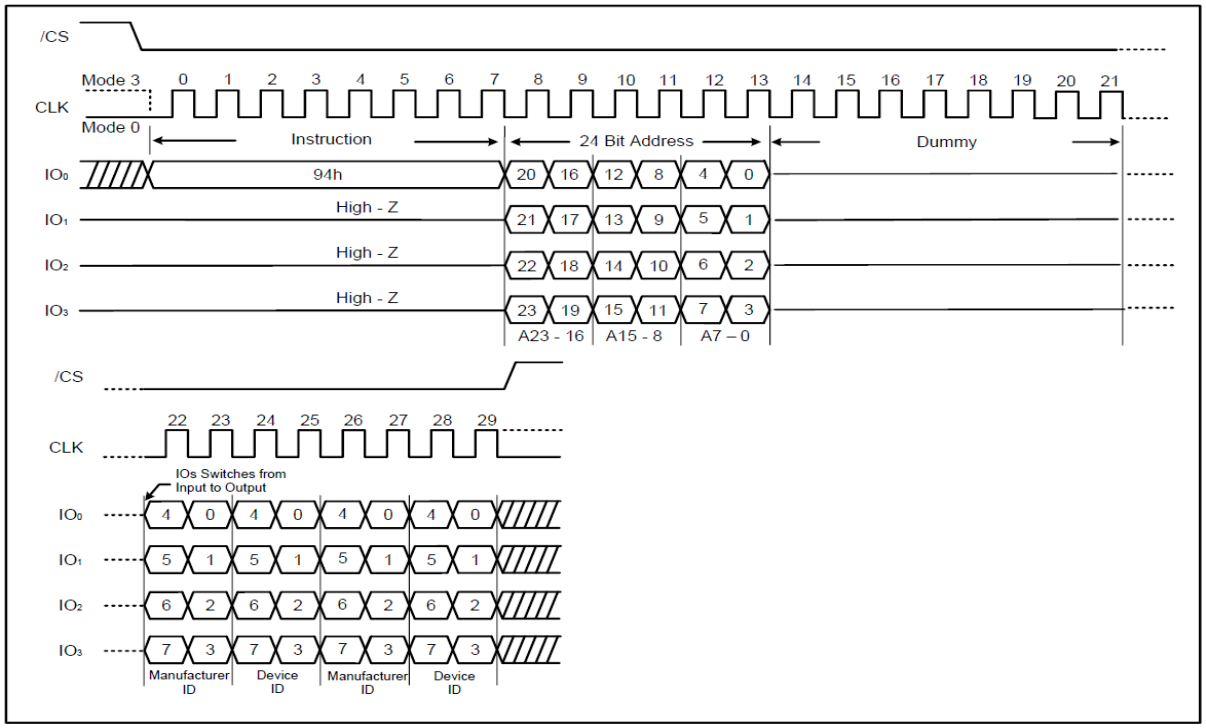


Figure 38. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

8.2.45. **Read JEDEC ID (9Fh)**

For compatibility reasons, the DS25Q4DN provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code "9Fh". The JEDEC assigned Manufacturer ID byte for Dosilicon (E5h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 39a & 39b. For memory type and capacity values refer to Manufacturer and Device Identification table.

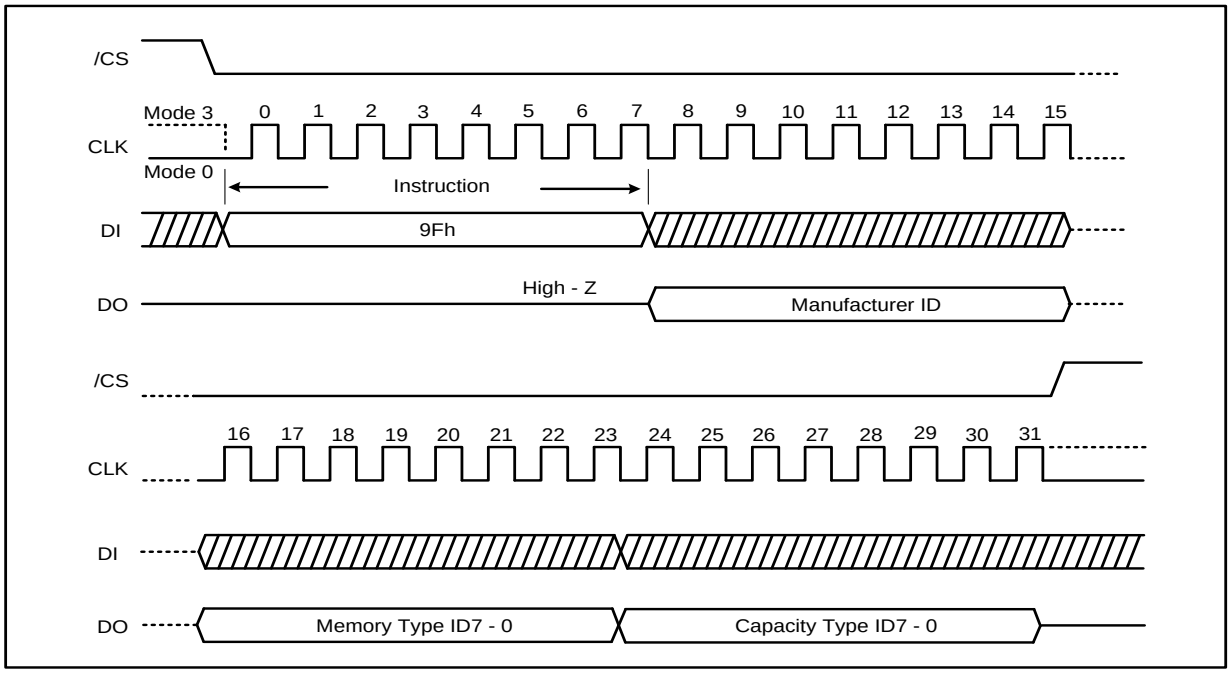


Figure 39a. Read JEDEC ID Instruction (SPI Mode)

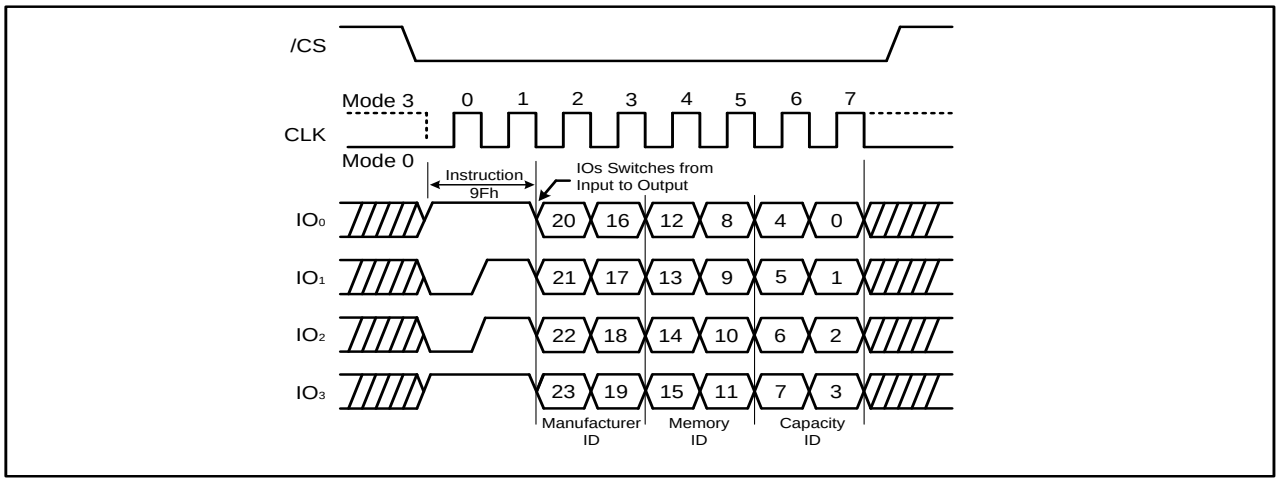


Figure 39b. Read JEDEC ID Instruction (QPI Mode)

8.2.46. **Read SFDP Register (5Ah)**

The DS25Q4DN features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0) of 000000h into the DI pin. Eight "dummy" clocks(SPI mode) are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 40a, 40b. For SFDP register values and descriptions, please refer to the Dosilicon Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

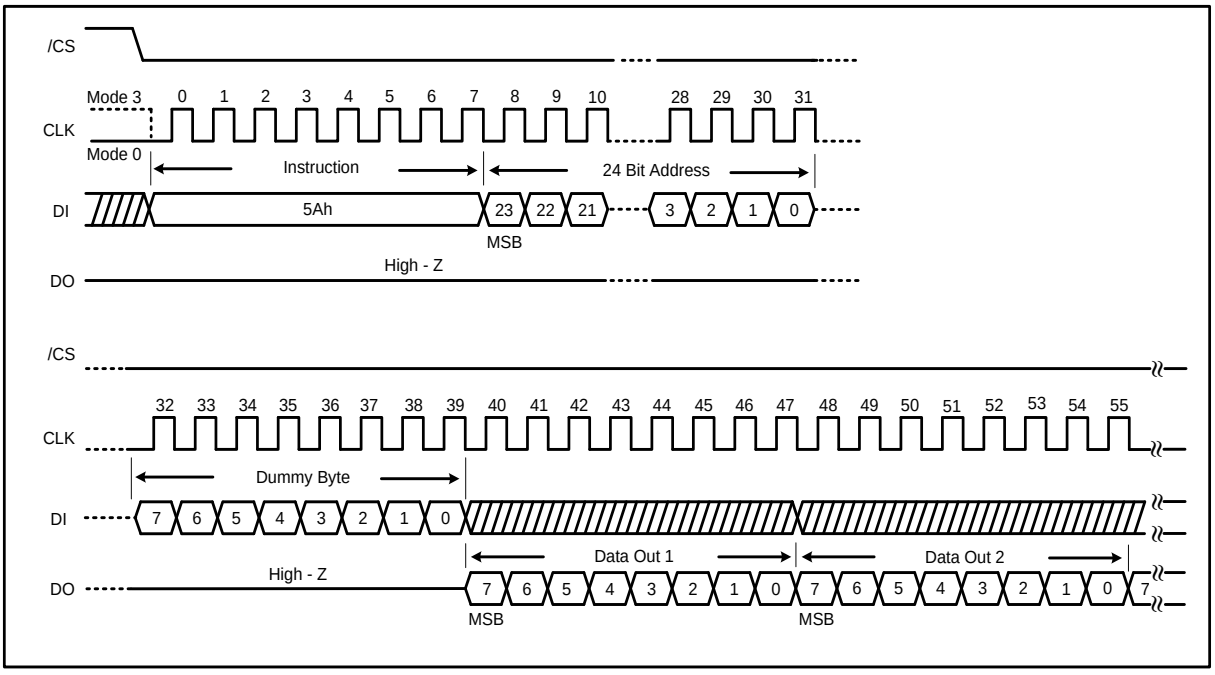


Figure 40a. Read SFDP Register Instruction Sequence Diagram

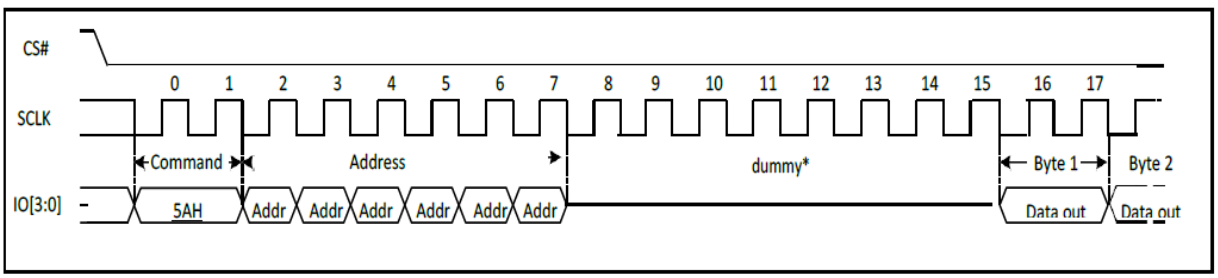


Figure 40b. Read SFDP Register Instruction Sequence Diagram (QPI Mode)

8.2.47. **Read Unique ID Number (4Bh)**

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each DS25Q4DN device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by 24 bits of '0' and one dummy byte. After which, the 128-bit ID is shifted out on the falling edge of CLK as shown in Figure 41a, 41b.

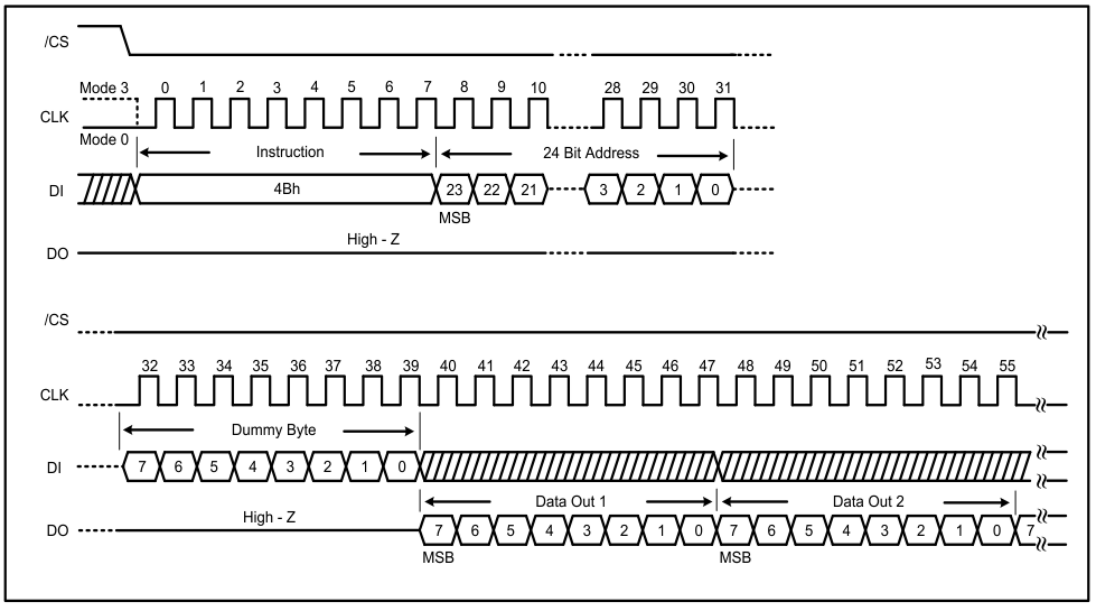


Figure 41a. Read Unique ID Number Instruction(SPI mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

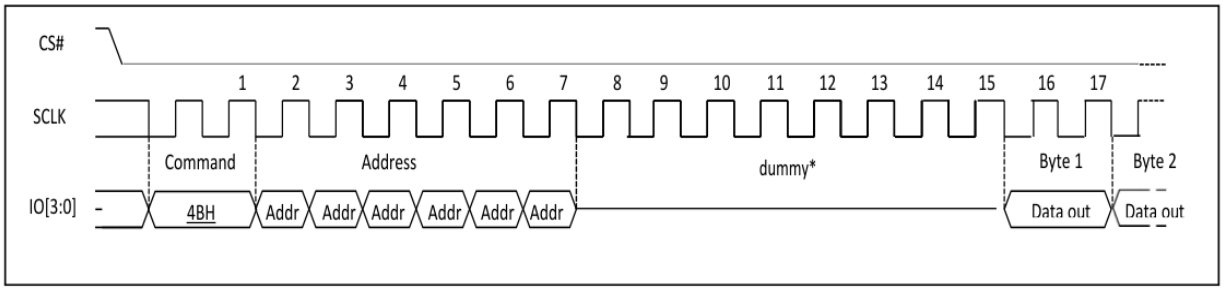


Figure 41b. Read Unique ID Number Instruction(QPI mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.48. **Erase Security Registers (44h)**

The DS25Q4DN offers 3x1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-A10	A9-0
Security Register #1	00h	0 0 0 1b	0 0b	Don't Care
Security Register #2	00h	0 0 1 0b	0 0b	Don't Care
Security Register #3	00h	0 0 1 1b	0 0b	Don't Care

The Erase Security Register instruction sequence is shown in Figure 42a, 42b. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 7.1.8 for detail descriptions).

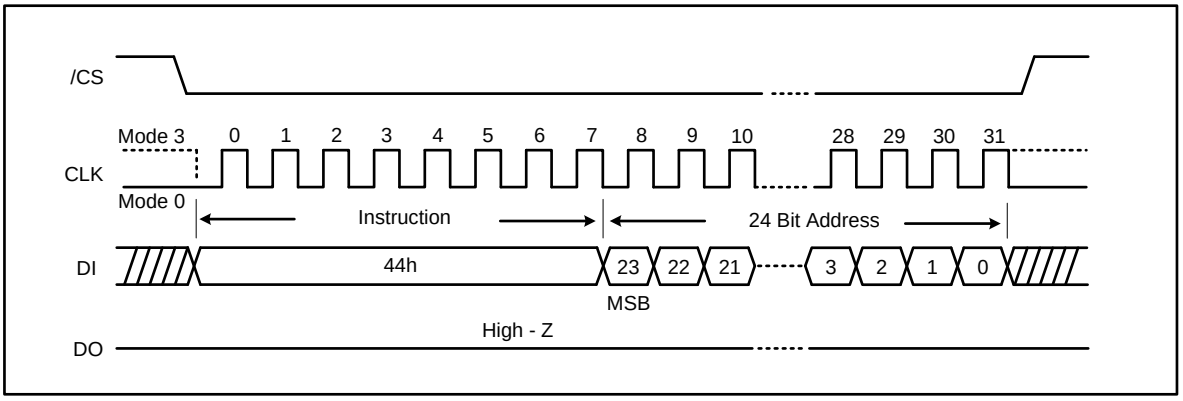


Figure 42a. Erase Security Registers Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

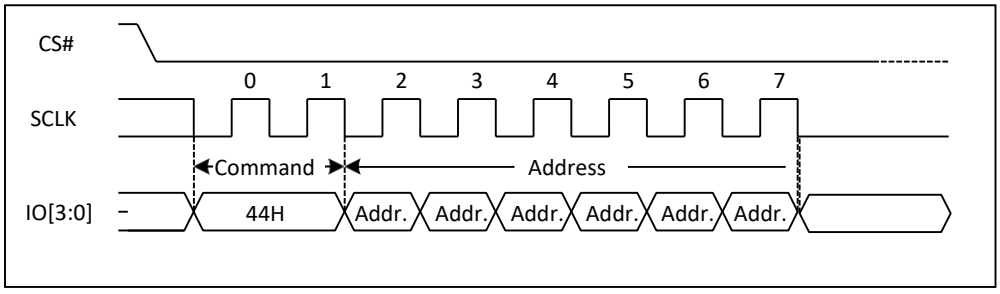


Figure 42b. Erase Security Registers Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit

8.2.49. Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 1024 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "42h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-A10	A9-0
Security Register #1	00h	0 0 0 1b	0 0b	Byte Address
Security Register #2	00h	0 0 1 0b	0 0b	Byte Address
Security Register #3	00h	0 0 1 1b	0 0b	Byte Address

The Program Security Register instruction sequence is shown in Figure 43a, 43b. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See Section "Security Register Lock Bits(LB3, B2, LB1) for detail descriptions). 43

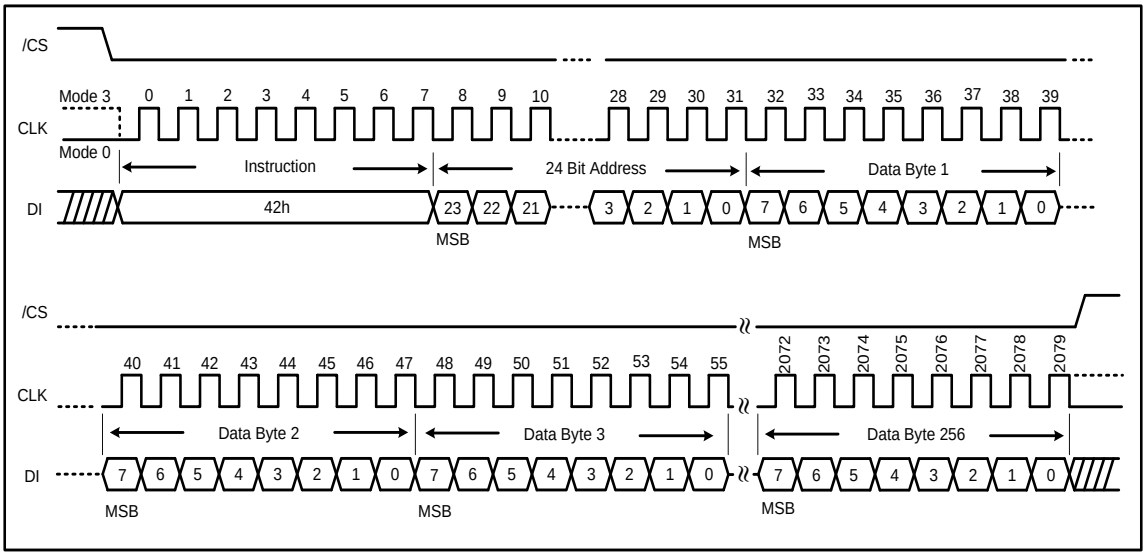


Figure 43a. Program Security Registers Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

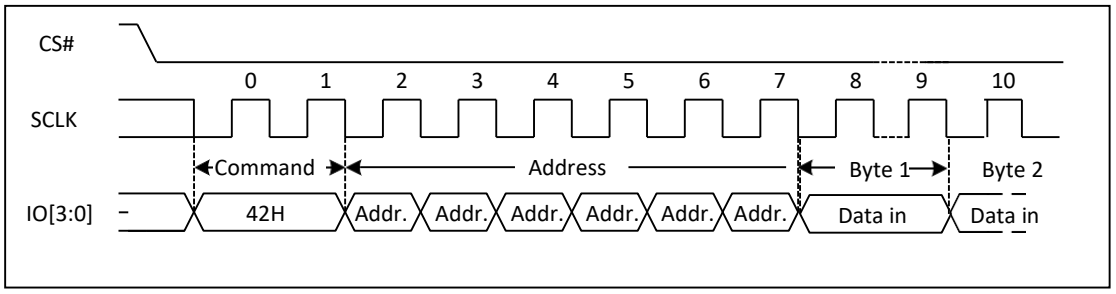


Figure 43b. Program Security Registers Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.50. **Read Security Registers (48h)**

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the 3 security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code "48h" followed by a 24-bit address (A23-A0) and eight "dummy" clocks(SPI mode) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address 3FFh), it will reset to address 000h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 44a, 44b. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of F_R (see AC Electrical Characteristics).

In QPI mode, the number of dummy clocks will be set by DC bits in configuration register, it can be configured as either 6/8/10/12/14/16 (default = 10).

ADDRESS	A23-16	A15-12	A11-A10	A9-0
Security Register #1	00h	0 0 0 1	0 0b	Byte Address
Security Register #2	00h	0 0 1 0	0 0b	Byte Address
Security Register #3	00h	0 0 1 1	0 0b	Byte Address

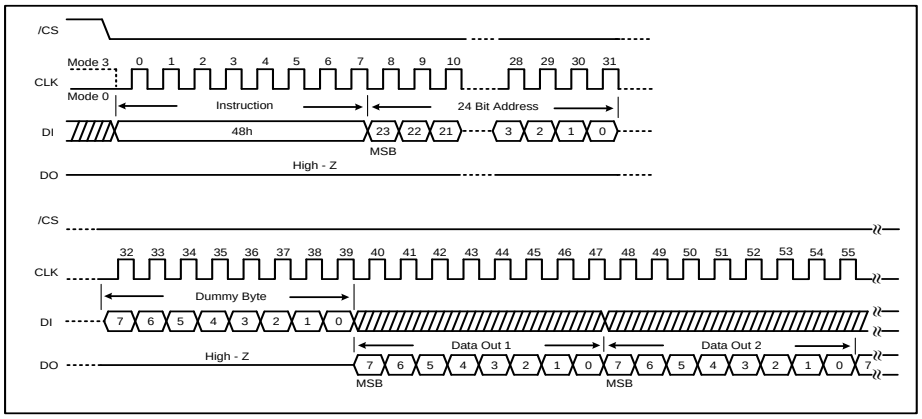


Figure 44a. Read Security Registers Instruction (SPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

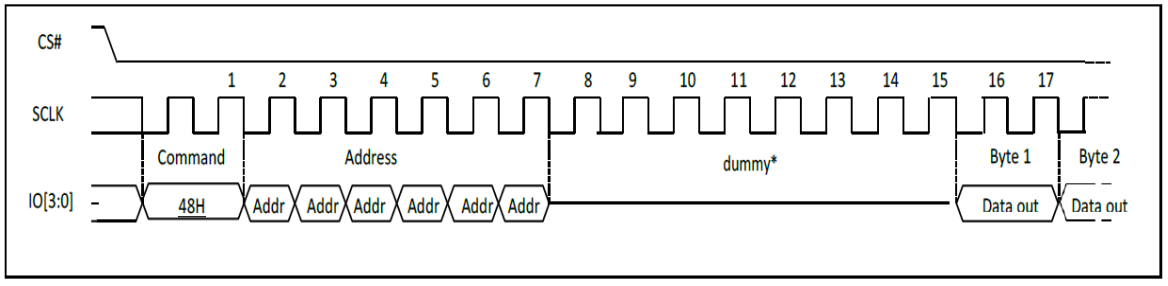


Figure 44b. Read Security Registers Instruction (QPI Mode)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.51. Individual Block/Sector Lock (36H)/Unlock (39H)/Read (3DH)

The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in status register 2 must be set to 1.

If WPS=0, the write protection will be determined by the combination of BP (4:0) bits in the Status Register.

The individual Block/Sector Lock command (36H) sequence: CS# goes low -> SI: Sending individual Block/Sector Lock command -> SI: Sending 3-Byte or 4-Byte individual Block/Sector Lock Address -> CS# goes high.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low -> SI: Sending individual Block/Sector Unlock command-> SI: Sending 3-Byte or 4-Byte individual Block/Sector Lock Address -> CS# goes high.

The Read individual Block/Sector lock command (3DH) sequence: CS# goes low -> SI: Sending Read individual Block/Sector Lock command -> SI: Sending 3-Byte or 4-Byte individual Block/Sector Lock Address -> SO: The Block/Sector Lock Bit will out -> CS# goes high. If the least significant bit (LSB) is1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

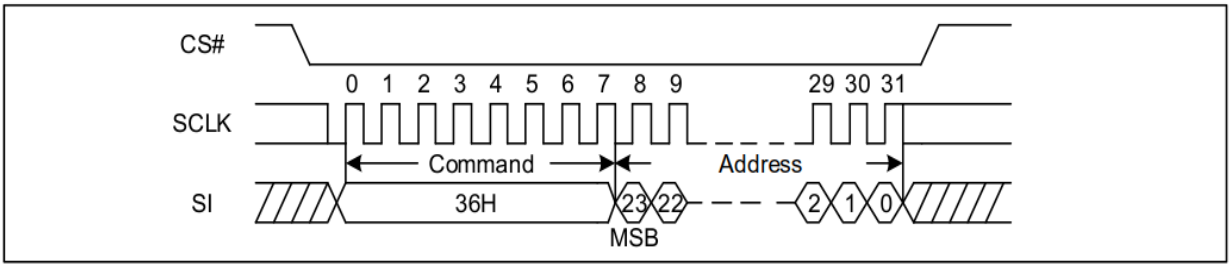


Figure 45a Individual Block/Sector Lock command Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

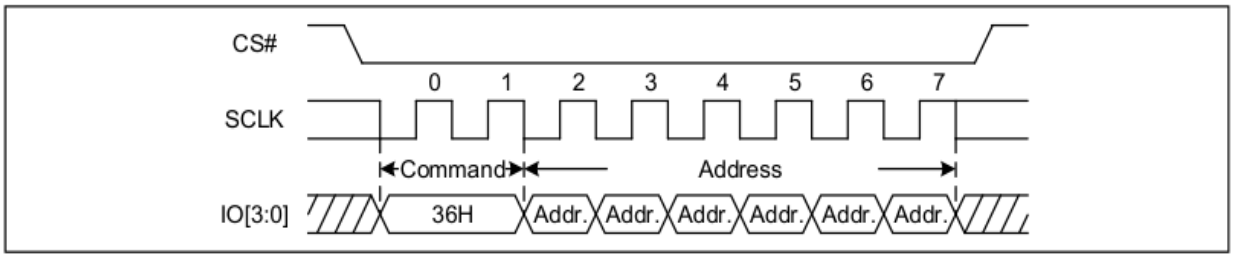


Figure 45b Individual Block/Sector Lock command Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

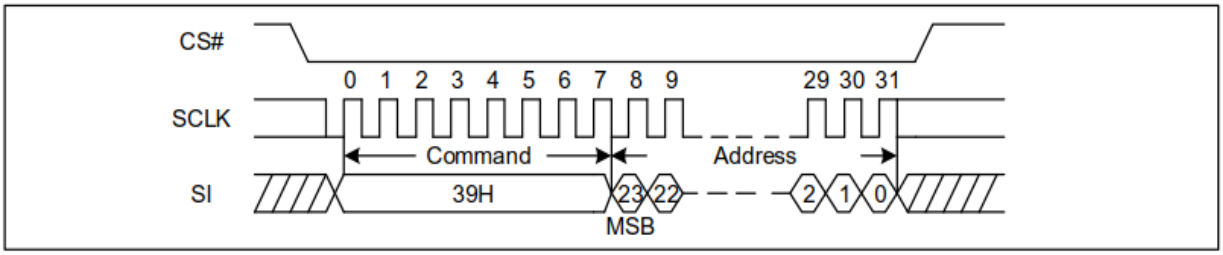


Figure 45c Individual Block/Sector Unlock command Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

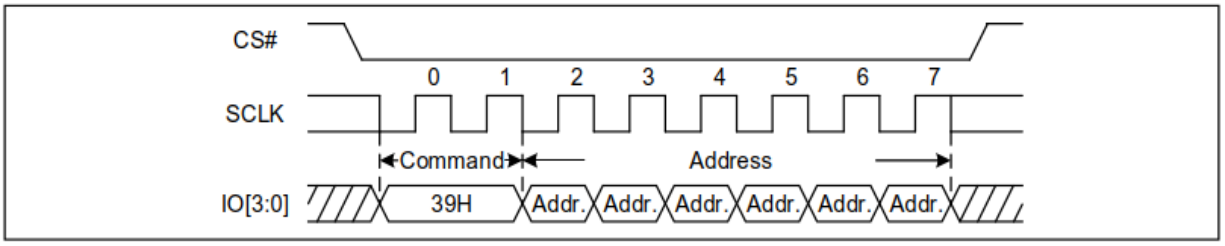


Figure 45d Individual Block/Sector Unlock command Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

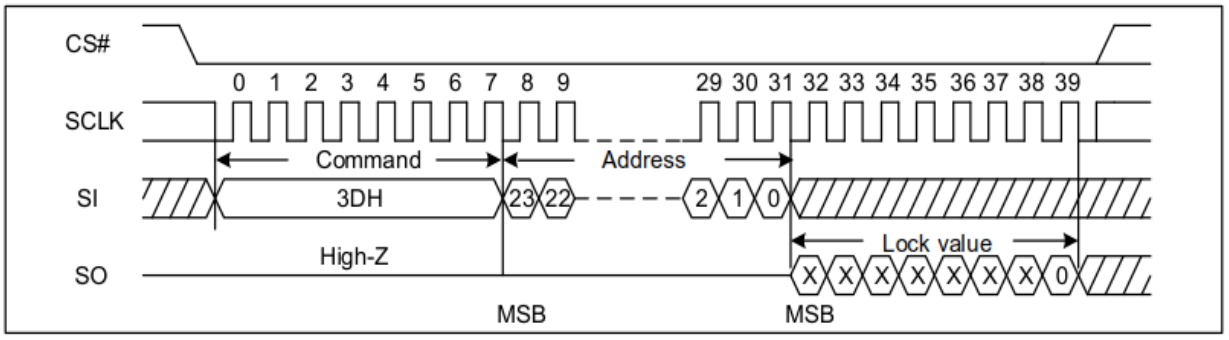


Figure 45e Read Individual Block/Sector lock command Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

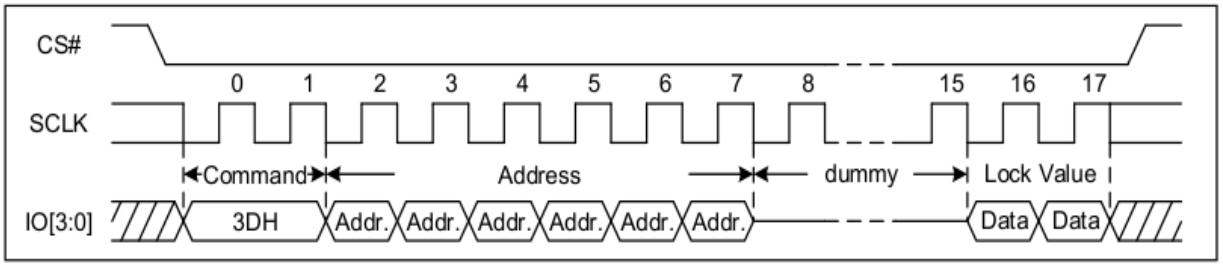


Figure 45f Read Individual Block/Sector lock command Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.52. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low -> SI: Sending Global Block/Sector Lock command -> CS# goes high.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low -> SI: Sending Global Block/Sector Unlock command -> CS# goes high.

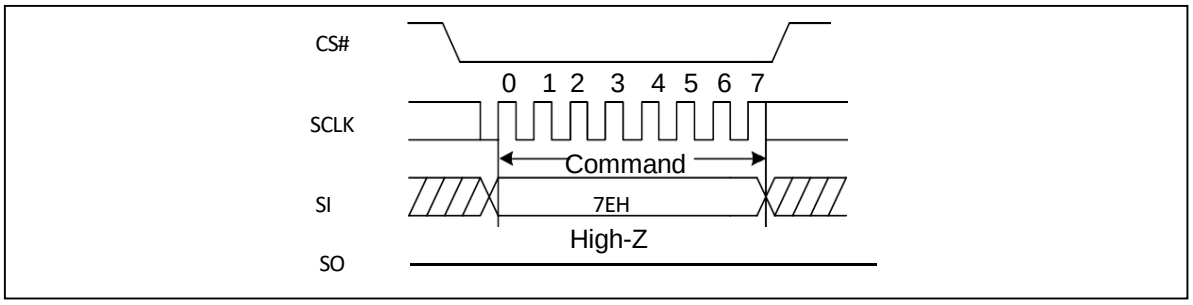


Figure 46a Global Block/Sector Lock Sequence Diagram (SPI)

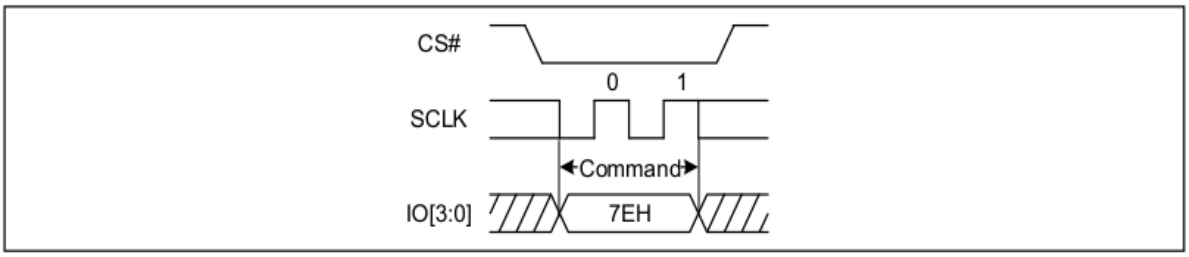


Figure 46b Global Block/Sector Lock Sequence Diagram (QPI)

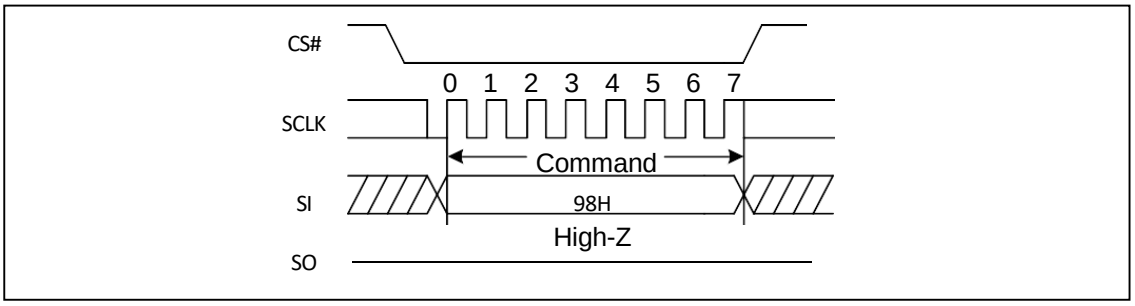


Figure 46c Global Block/Sector Unlock Sequence Diagram (SPI)

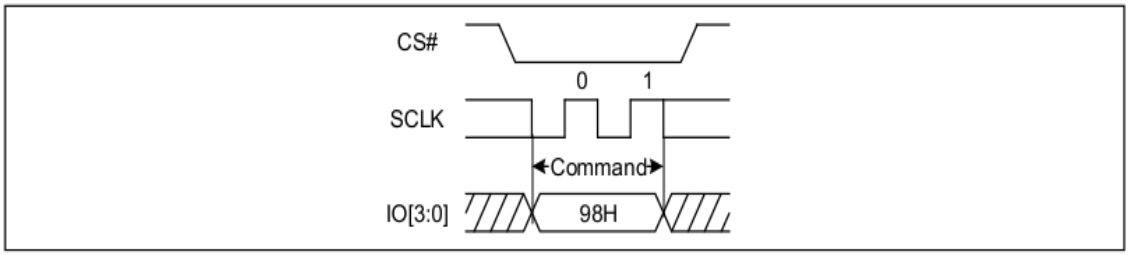


Figure 46d Global Block/Sector Unlock Sequence Diagram (QPI)

8.2.53. **Read Password (27h)**

Read Password instruction(27h) is initiated by driving the /CS pin low and shifting the instruction code "27h" followed by a 24-bit address (A23-A0). After which, 8 dummy clock and the 1 to 64-bit password is shifted out on the falling edge of CLK as shown in Figure 47a, 47b. Password can only be read out when PWDLK bit equals 1(factory default) as password lock is disable

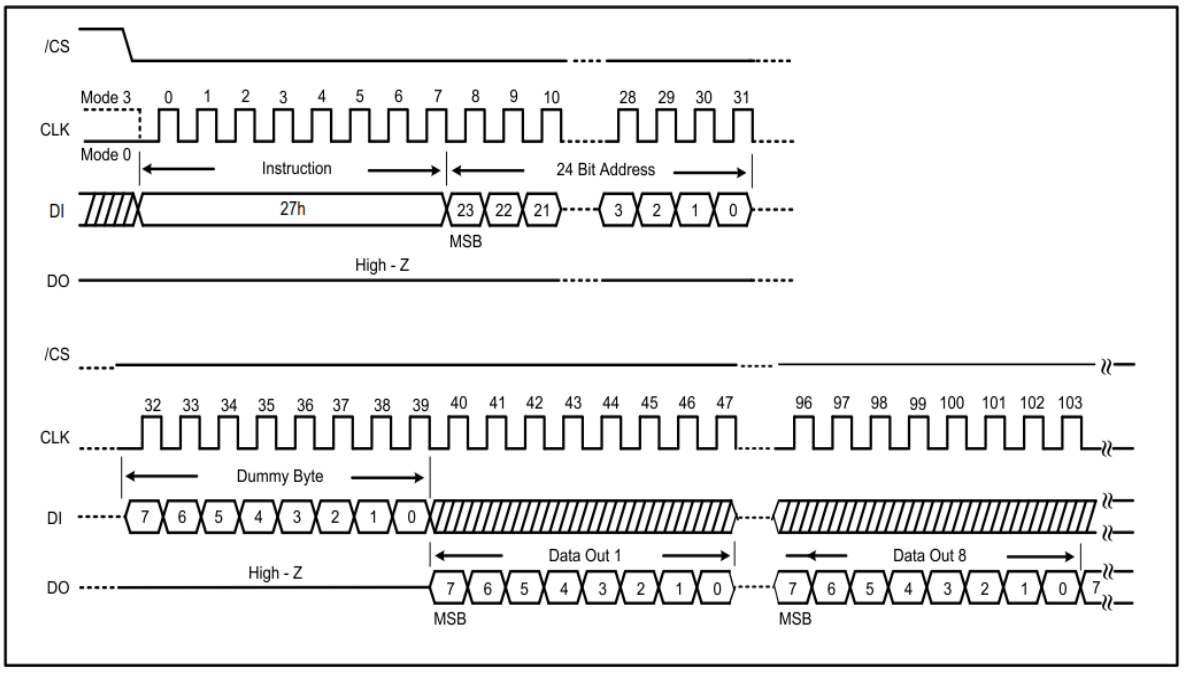


Figure 47a Read Password Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

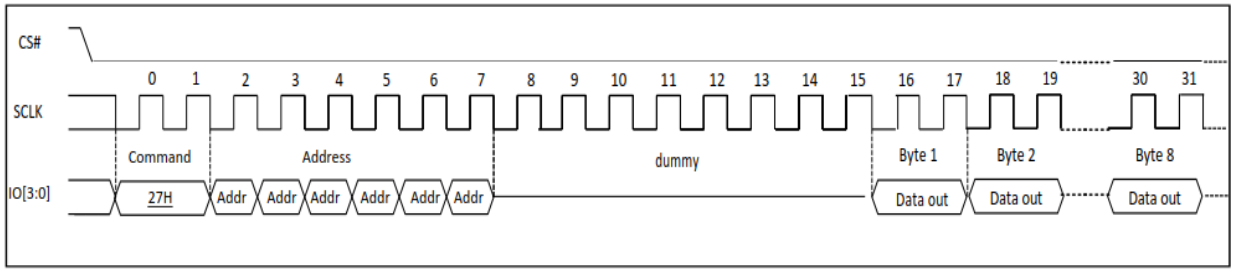


Figure 47b Read Password Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.54. **Write Password (28h)**

Write Password Register instruction(28h) is initiated by driving the /CS pin low and shifting the instruction code "28h" followed by a 24-bit address (A23-A0) and 1 to 64-bit password in to the DI pin as shown in Figure 48a, 48b. Password can only be written when PWDLK bit equals 1(factory default) as password lock is disable. A Write Enable instruction must be executed before this Write Password Register instruction.

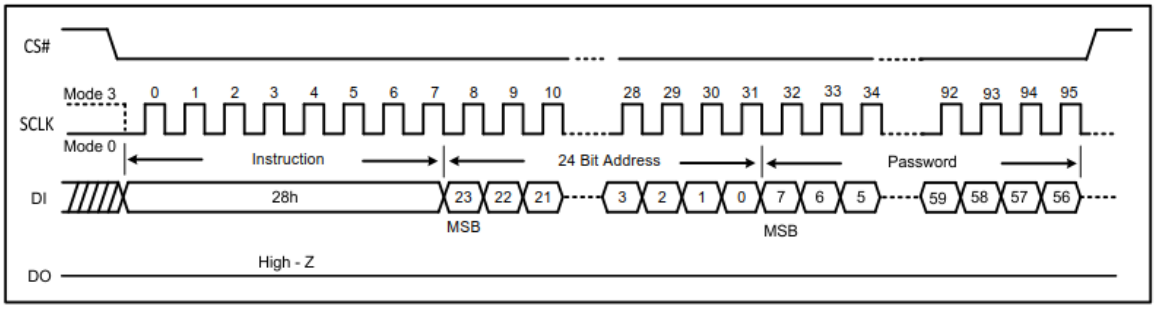


Figure 48a Write Password Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

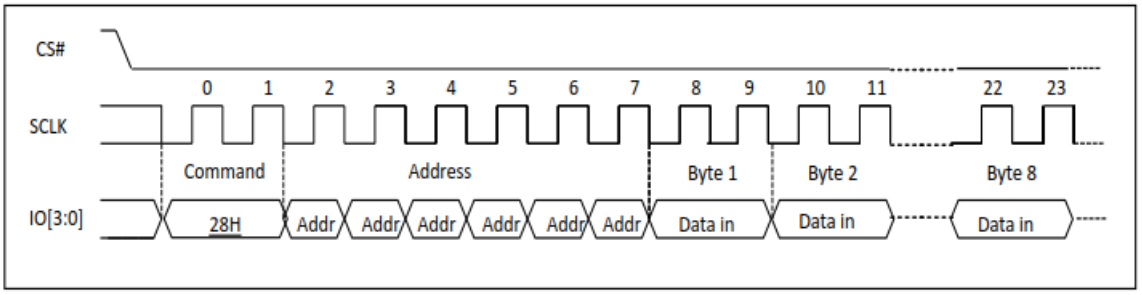


Figure 48b Write Password Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.55. **Unlock Password (29h)**

Unlock Password instruction(29h) is initiated by driving the /CS pin low and shifting the instruction code “29h” followed by a 24-bit address (A23-A0), 8 dummy clock and 1 to 64-bit password in to the DI pin as shown in Figure 49a, 49b. After unlock with correct password, global freeze bit automatically reset to 0, so that Individual/Global Block/Sector Lock/Unlock command can be used to change the Individual Block Protection bits in password protection mode.

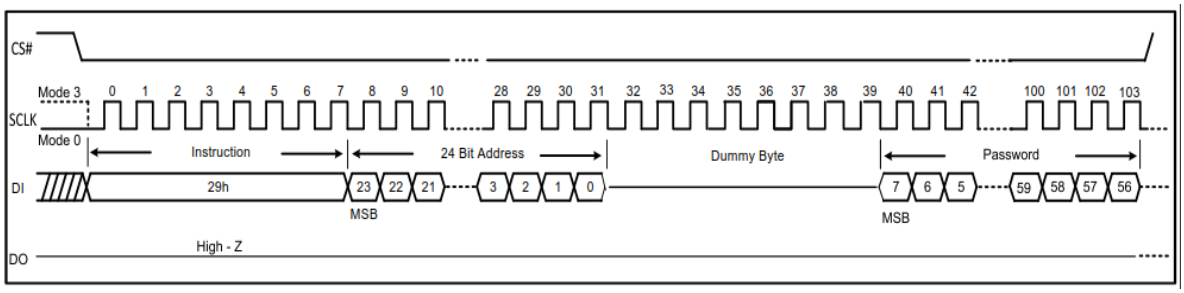


Figure 49a Unlock Password Sequence Diagram (SPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

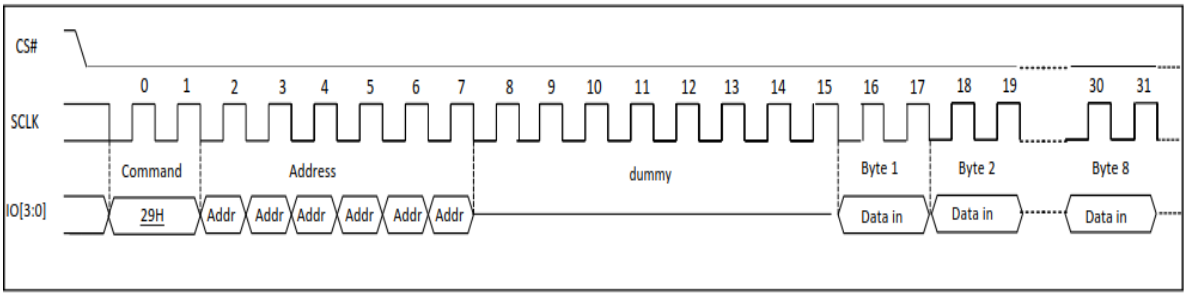


Figure 49b Unlock Password Sequence Diagram (QPI)

Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

8.2.56. **Read global freeze bit (A7h)**

Read global freeze bit instruction(A7h) is initiated by driving the /CS pin low and shifting the instruction code “A7h”, After which, the 1 byte data contains global freeze bit is shifted out on the falling edge of CLK as shown in Figure 50a, 50b. Bit 0 shows the value of global freeze bit and ignore other bits(1-7).

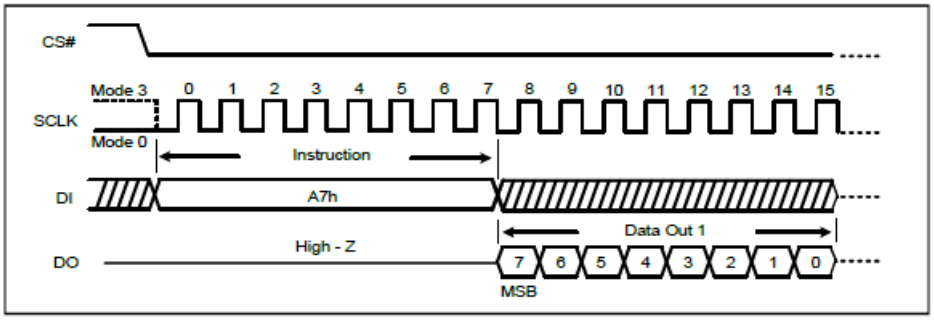


Figure 50a Read global freeze bit Sequence Diagram (SPI)

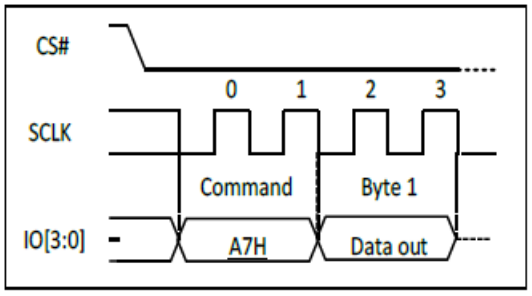


Figure 50b Read global freeze bit Sequence Diagram (QPI)

8.2.57. **Write global freeze bit (A6h)**

Write global freeze bit instruction(A6h) is initiated by driving the /CS pin low and shifting the instruction code “A6h” as shown in Figure 51, Note that Write global freeze bit instruction(A6h) can only set global freeze bit to 1 so that the Individual Block Protection bits can not be modify without password to unlock again in password protection mode. A Write Enable instruction must be executed before this Write global freeze bit instruction.

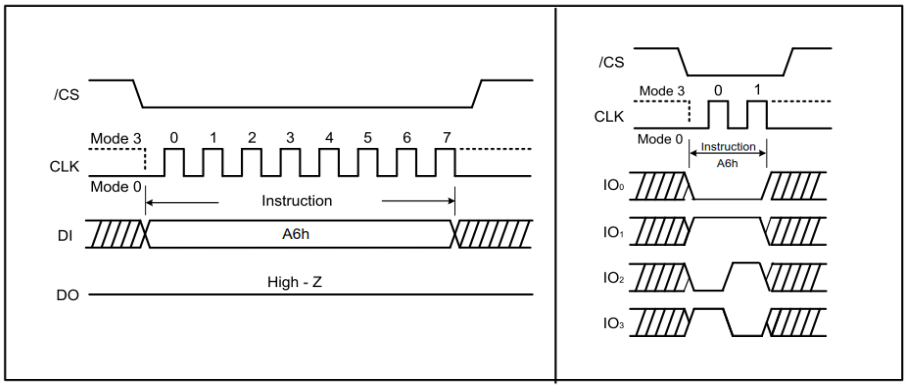


Figure 51 Write global freeze bit Sequence Diagram (SPI/QPI)

8.2.58. **Set Read Parameters (C0h)**

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of bytes of “Wrap Length” for “Quad I/O Fast Read (EBH/ECH)” and “DTR Fast Read Quad I/O (EDH/EEH)” instruction.

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The default “Wrap Length” after a power up or a Reset instruction is 16 bytes.

P2	P1 – P0	WRAP LENGTH
Enable wrap =0	0 0	16-byte
Disable wrap =1(Default)	0 1	16-byte
	1 0	32-byte
	1 1	64-byte

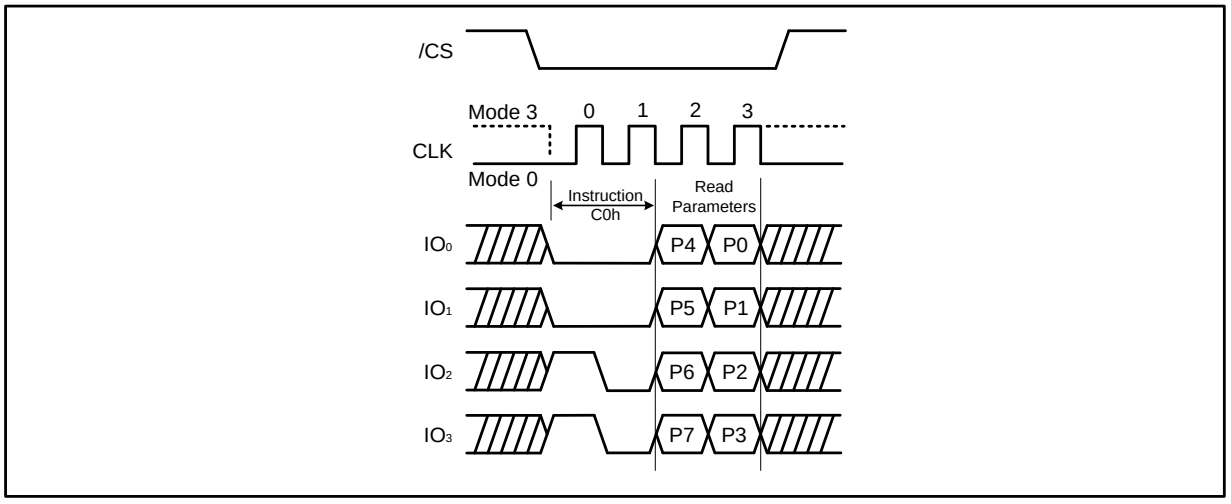


Figure 52 Set Read Parameters Instruction (QPI Mode only)

8.2.59. **Enter QPI Mode (38h)**

The DS25Q4DN support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Dosilicon serial flash memories. See Instruction Set Table 1-3 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 3 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

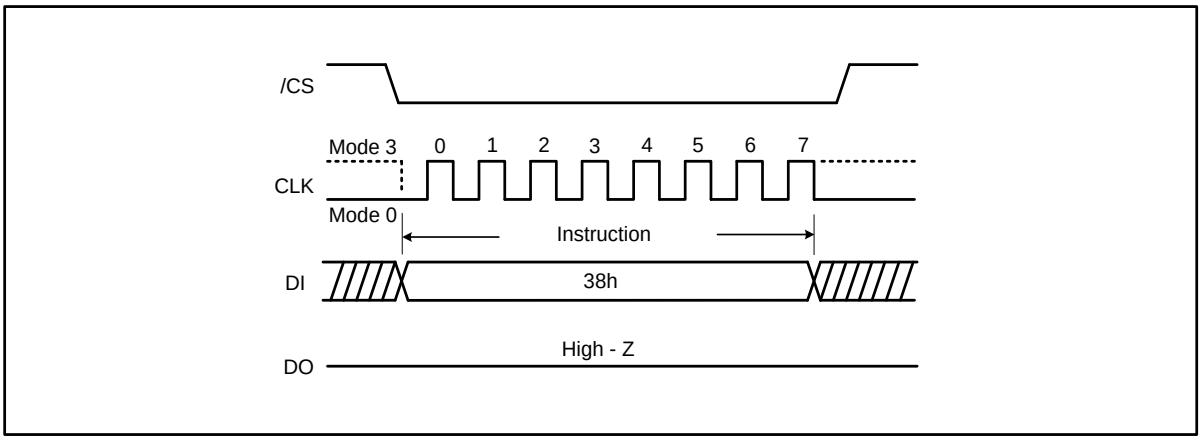


Figure 53. Enter QPI Instruction (SPI Mode only)

8.2.60. **Exit QPI Mode (FFh)**

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

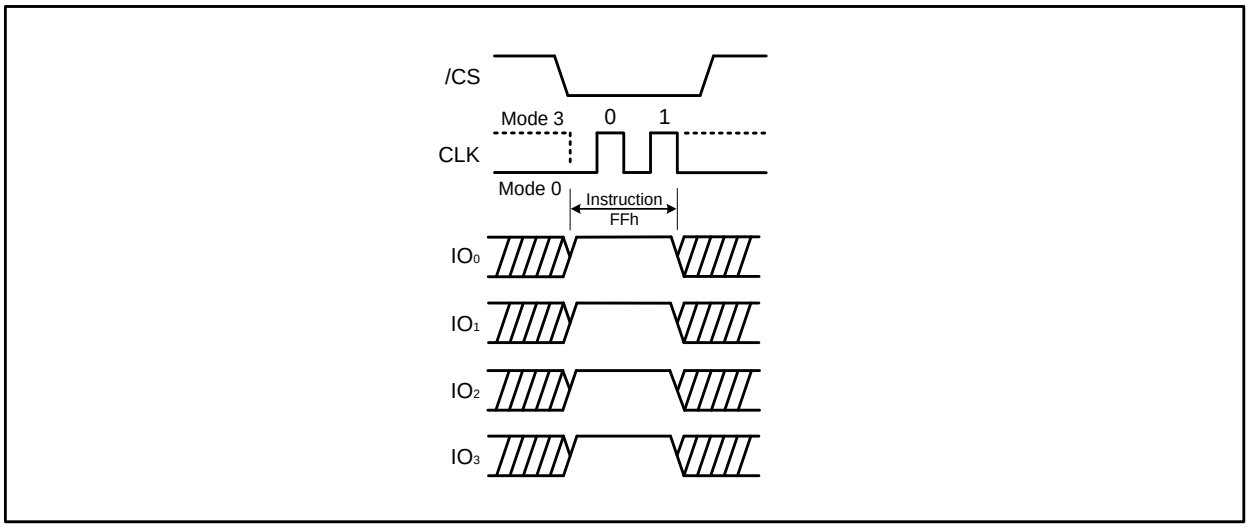


Figure 54. Exit QPI Instruction (QPI Mode only)

8.2.61. Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the DS25Q4DN provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting(W6-W4).

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=40us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

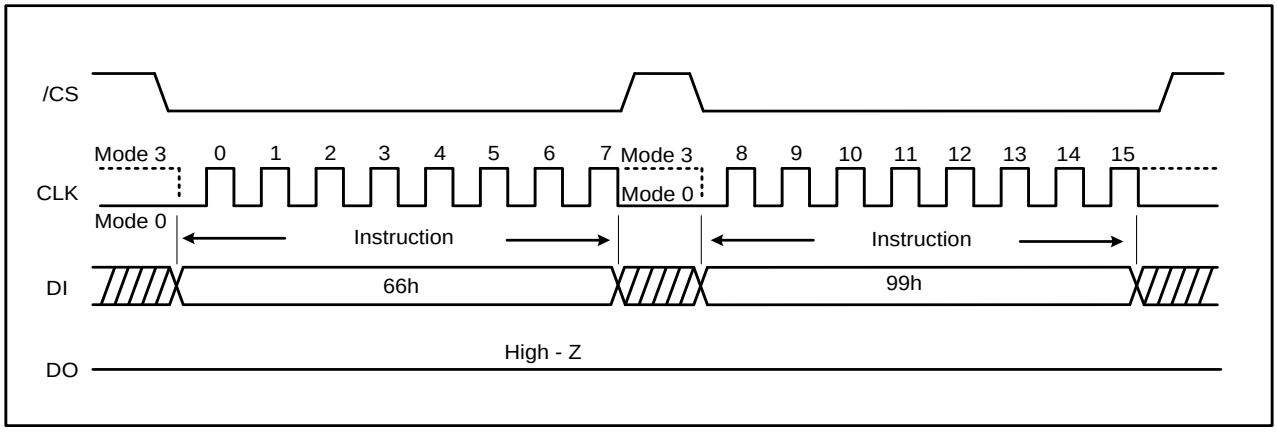


Figure 55a. Enable Reset and Reset Instruction Sequence (SPI Mode)

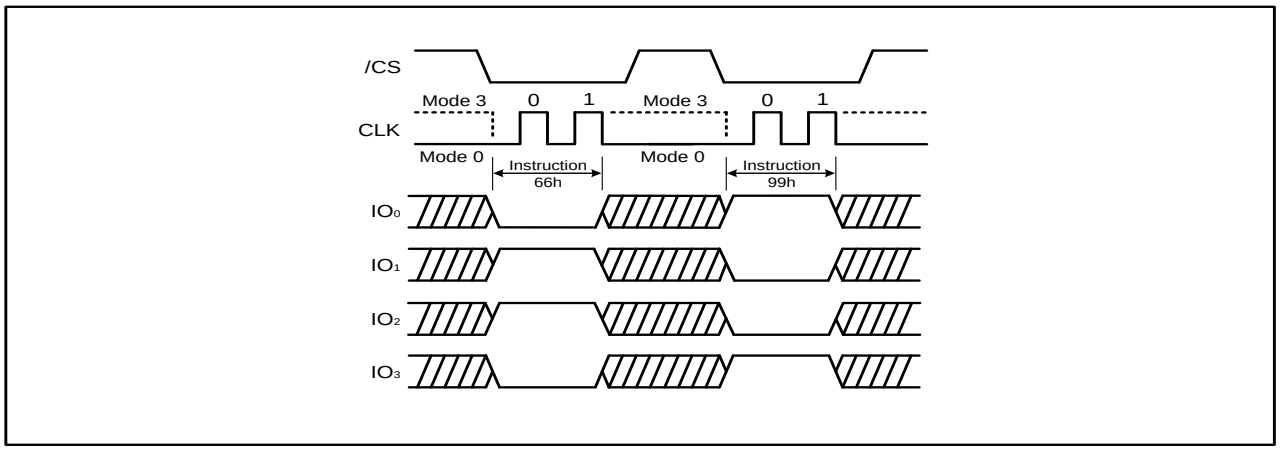


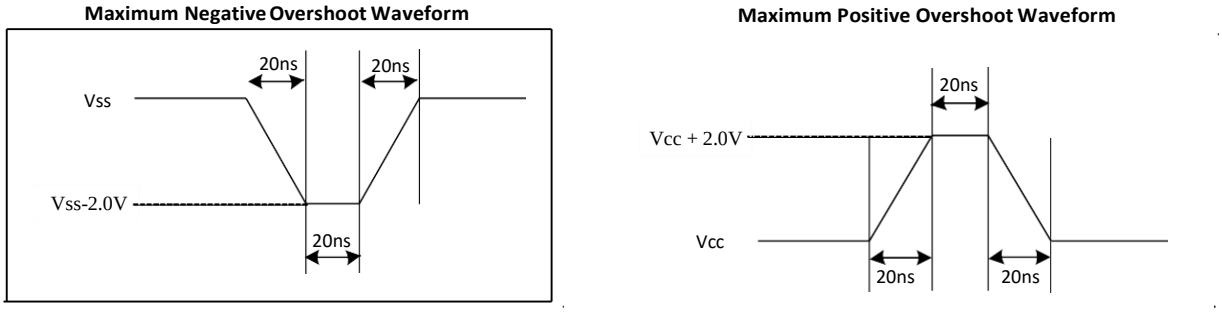
Figure 55b. Enable Reset and Reset Instruction Sequence (QPI Mode)

9. ELECTRICAL CHARACTERISTICS

9.1. Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85/105/125	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.5	V
VCC	-0.6 to 4.2	V

Figure 56. Input Test Waveform and Measurement Level



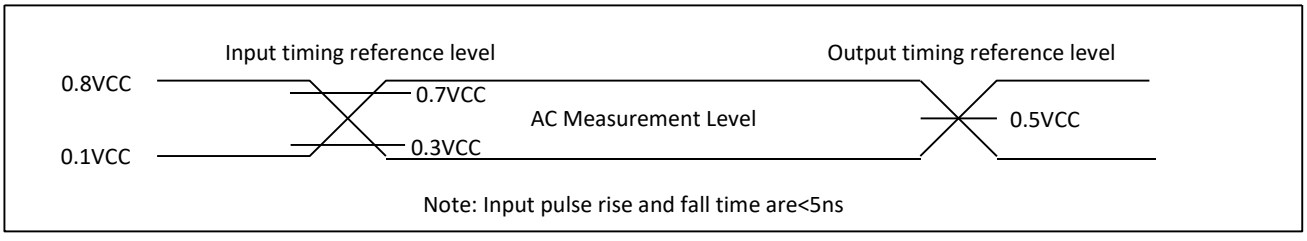
9.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). All Status Register bits are set to 0 except DRV1(DRV1 equals to 1).

9.3. Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pause Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.3VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 57. Absolute Maximum Ratings Diagram



9.4. Power-Up Timing and Requirements

Figure 58. Power-On Timing Sequence Diagram

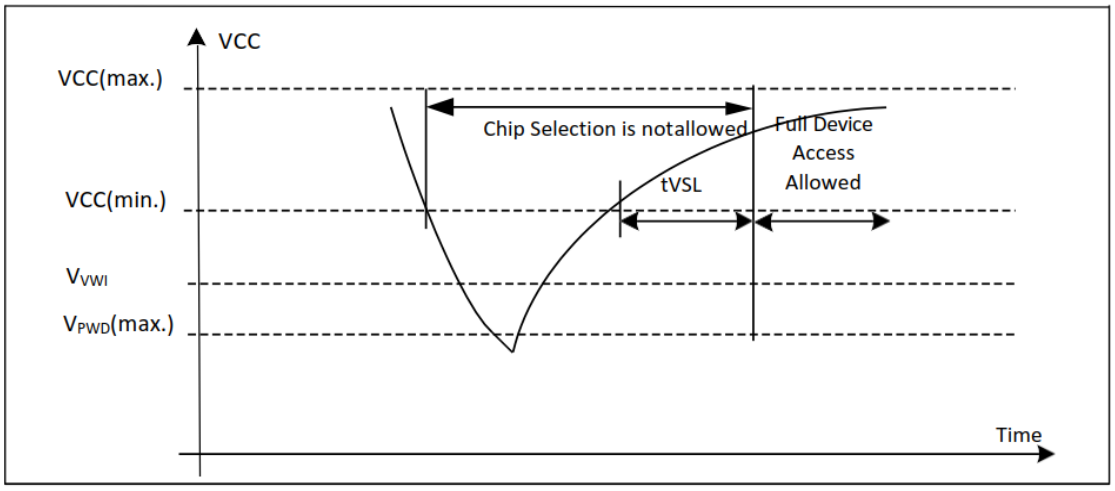


Table 17. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	200		μs
VWI	Write Inhibit Voltage	1.5	2.5	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.4	V

9.5. DC Electrical Characteristics

(T_A = -40℃~85℃/105℃/125℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		25	80/120/240	uA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	15/30/50	uA
I_{CC3}	Operating Current (Read)	90M Q=Open(X4IO) DTR		16	20/25/28	mA
		104M Q=Open(X4IO)		15	20/25/30	mA
		133M Q=Open(X4IO)		19	25/30/35	mA
		166M Q=Open(X4IO)		24	35/40/45	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		17	25/30/35	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		10	20/25/30	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		10	15/20/25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	15/20/25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		25	35/40/45	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 3.3V. X/X/X means values of 85℃/105℃/125℃ product
2. Value guaranteed by design and/or characterization, not 100% tested in production

9.6. AC Electrical Characteristics

(T_A = -40℃~85℃/105℃/125℃, VCC=2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_{C1}	Serial Clock Frequency for: all commands except normal Read and DTR read (normal read: 03H,13H DTR read: EDH,EEH)			166	MHz
f_{C2}	Serial Clock Frequency for DTR Read (DTR read: EDH,EEH)			90	MHz
f_R	Serial Clock Frequency For: Read (03H,13H)			60	MHz
t_{CLH}	Serial Clock High Time	45%(1/Fc)			ns
t_{CLL}	Serial Clock Low Time	45%(1/Fc)			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.3			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.3			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{CLSH}	CS# Active Hold Time (DTR)	5			
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20/40			ns
t_{SHQZ}	Output Disable Time			8	ns
t_{CLQX}/ t_{CHQX}	Output Hold Time	1			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{ECSV}	ECS# Setup Time			10	ns
t_{CLQV}	Clock Low To Output Valid (CL = 30pF)			7	ns
	Clock Low To Output Valid (CL = 12pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	µs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	µs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	µs
t_{SUS}	CS# High To Next Command After Suspend			30	µs
t_{RS}	Latency Between Resume And Next Suspend	100			µs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			40	µs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			25	ms

t_W	Write Status Register Cycle Time		5	30/40/40	ms
t_{PP}	Page Programming Time		0.3	1/2/2	ms
t_{SE}	Sector Erase Time(Industrial)		30	400/600/800	ms
	Sector Erase Time(Automotive)		85	400/600/800	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.15	1.5/1.6/1.6	s
t_{BE2}	Block Erase Time (64K Bytes)		0.22	2/3/3	s
t_{CE}	Chip Erase Time (DS25Q4DN)		60	100	s

Note:

1. Typical value at T_A=25℃, X/X/X means values of 85℃/105℃/125℃ product.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. If STR frequency exceeds 166MHz or DTR frequency exceeds 90MHz, please contact us.

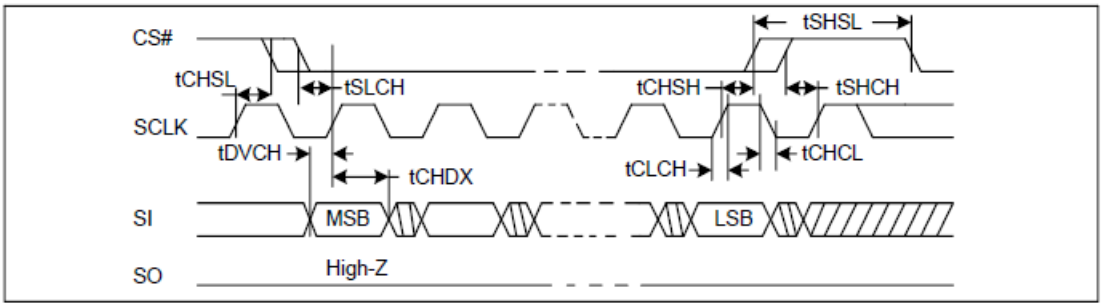


Figure 59. Input Timing

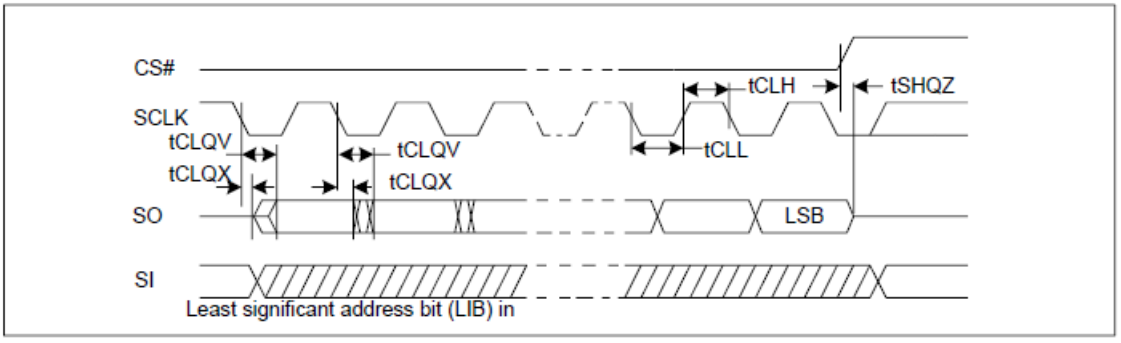


Figure 60. Output Timing

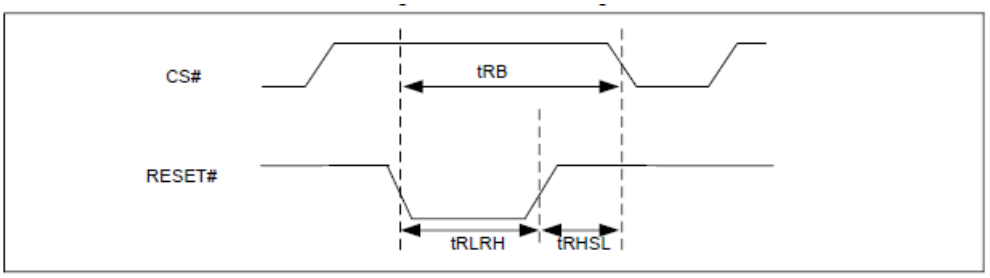
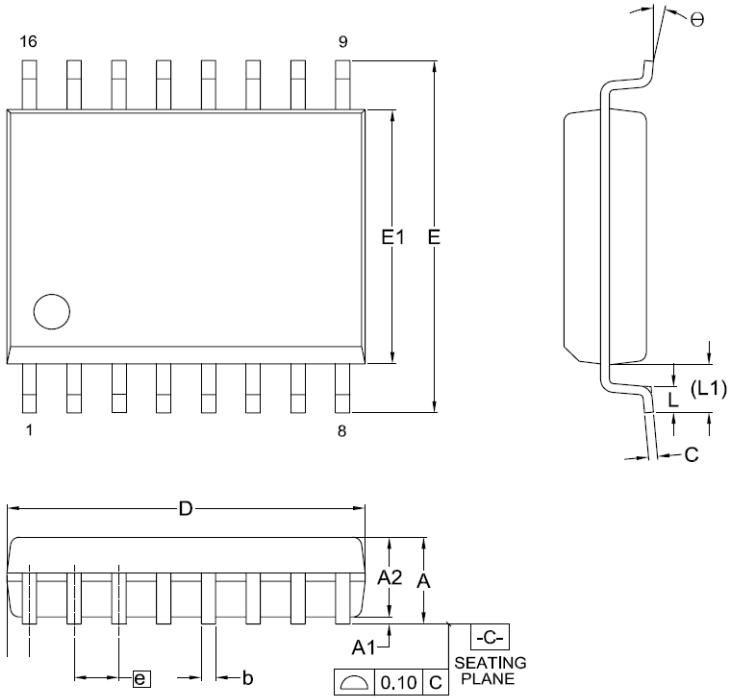


Figure 61. Reset Timing

Symbol	Parameter	Min.	Typ.	Max	Unit.
t_{RLRH}(t_{RESET})	Reset Pulse Width	1			μs
t_{RHSL}	Reset Hold time before next Operation	40			ns
t_{RB}	Reset Recovery Time (From Read or Program)			40	μs
	Reset Recovery Time (From Erase)			25	ms

10. PACKAGE SPECIFICATIONS

10.1. 16-pin SOP 300-mil

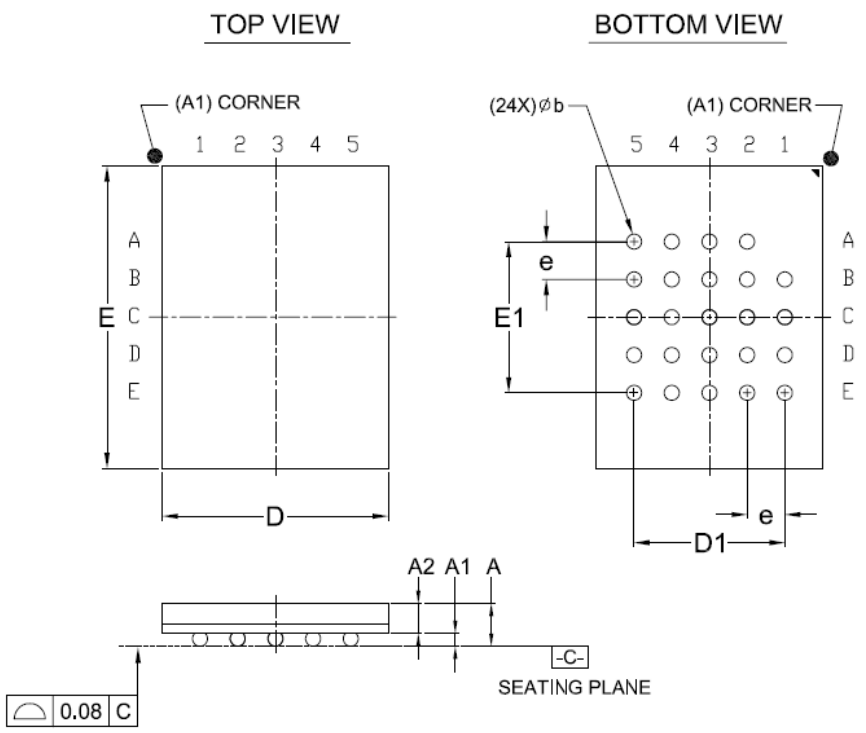


SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A			2.65			0.104
A1	0.10	0.20	0.30	0.004	0.008	0.012
A2	2.25	2.30	2.35	0.089	0.091	0.093
b	0.35		0.43	0.014		0.017
C	0.25		0.31	0.010		0.012
D	10.20	10.30	10.40	0.402	0.406	0.410
E	10.20	10.30	10.40	0.402	0.406	0.410
E1	7.40	7.50	7.60	0.292	0.296	0.299
e	1.27 BSC			0.050 BSC		
L	0.55	0.70	0.85	0.022	0.028	0.034
L1	1.40REF			0.055REF		
Θ	0°	-	8°	0°	-	8°
Seating Plane	-	-	0.10	-	-	0.004

Notes:

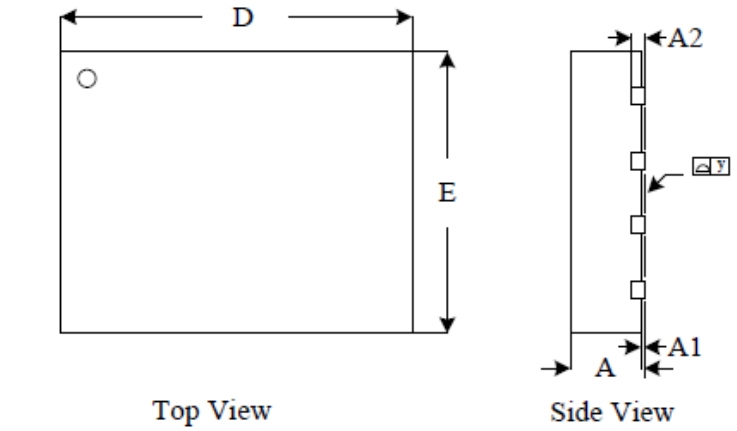
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

10.2. **24Ball FBGA**



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.20			0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.65			0.026		
b	0.35	0.40	0.45	0.014	0.16	0.018
D	5.90	6.00	6.10	0.232	0.236	0.240
D1		4.00			0.157	
E	7.90	8.00	8.10	0.311	0.315	0.319
E1		4.00			0.157	
e	1.00BSC			0.039BSC		

10.3. **WSON(8*6mm)**



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.70			0.35	7.95	3.25	5.95	4.15		0.00	0.40
	Nom	0.75		0.20	0.40	8.00	3.40	6.00	4.30	1.27		0.50
	Max	0.80	0.05		0.45	8.05	3.50	6.05	4.40		0.05	0.60
Inch	Min	0.028			0.014	0.313	0.128	0.234	0.163		0.00	0.016
	Nom	0.030		0.008	0.016	0.315	0.134	0.236	0.169	0.05		0.020
	Max	0.032	0.002		0.019	0.317	0.138	0.238	0.173		0.002	0.024

11. ORDERING INFORMATION